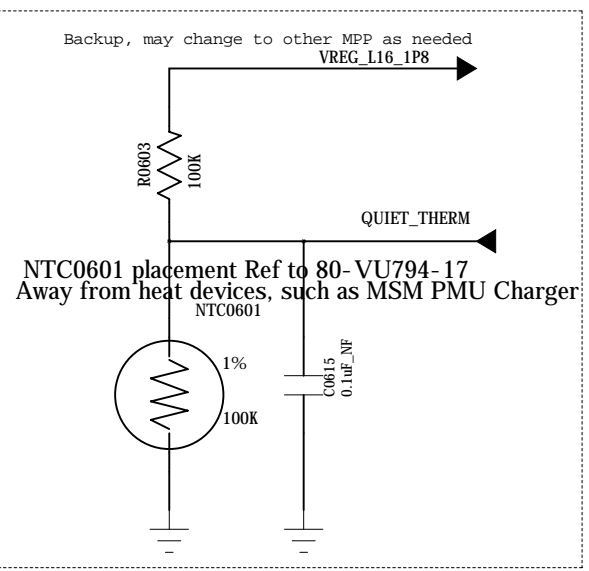
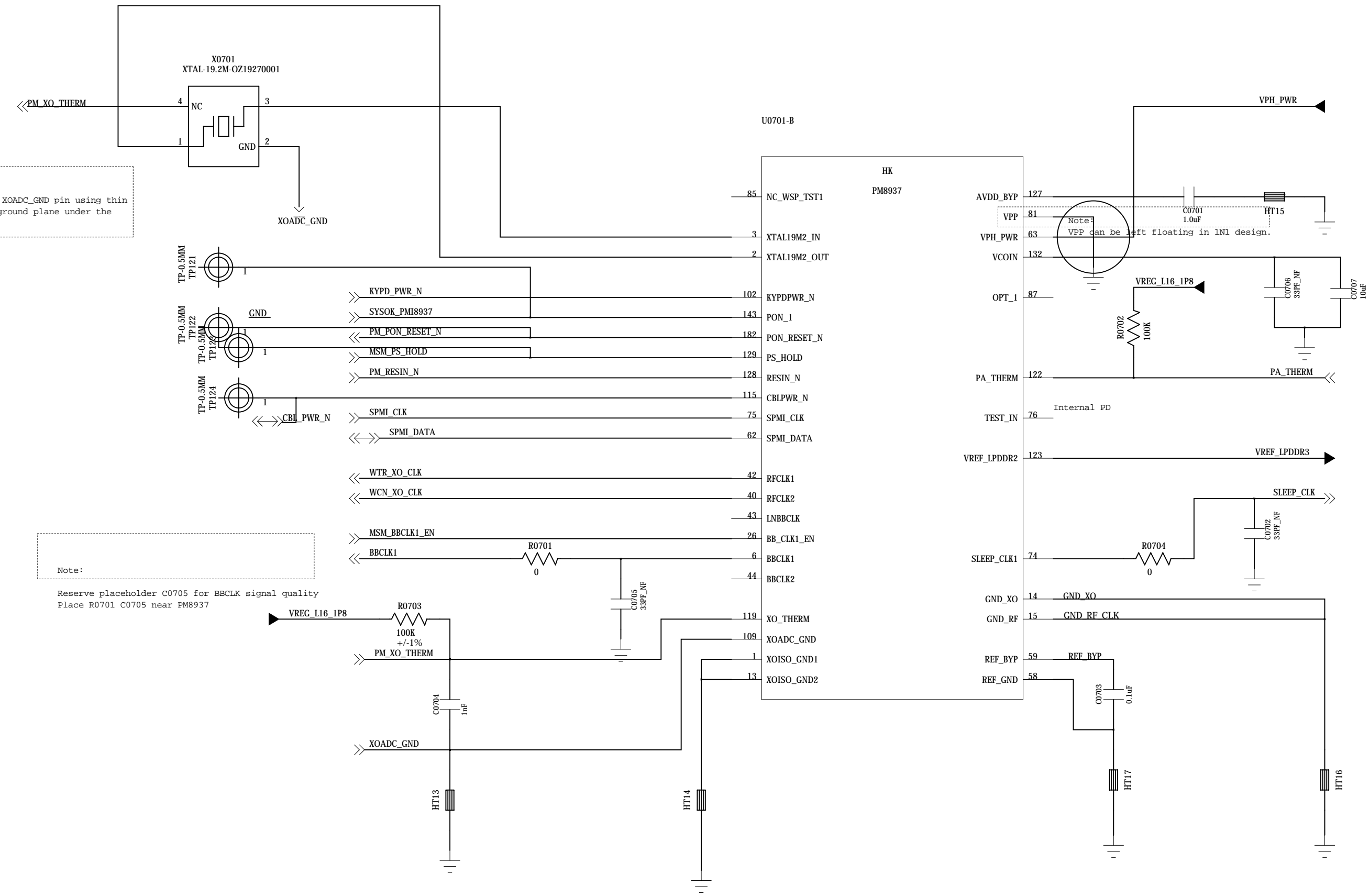


PMI8937 CHARGER

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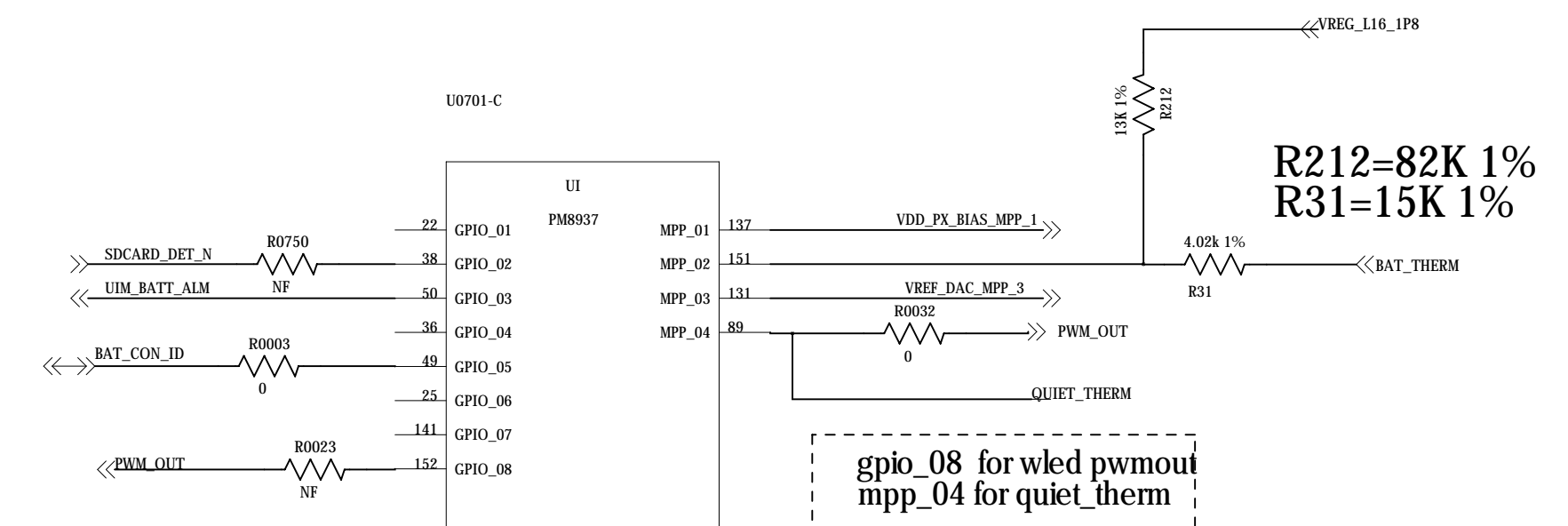


Note:
XO GND should connect to XOADC_GND pin using thin traces, then via to main ground plane under the XO_THERM cap ground

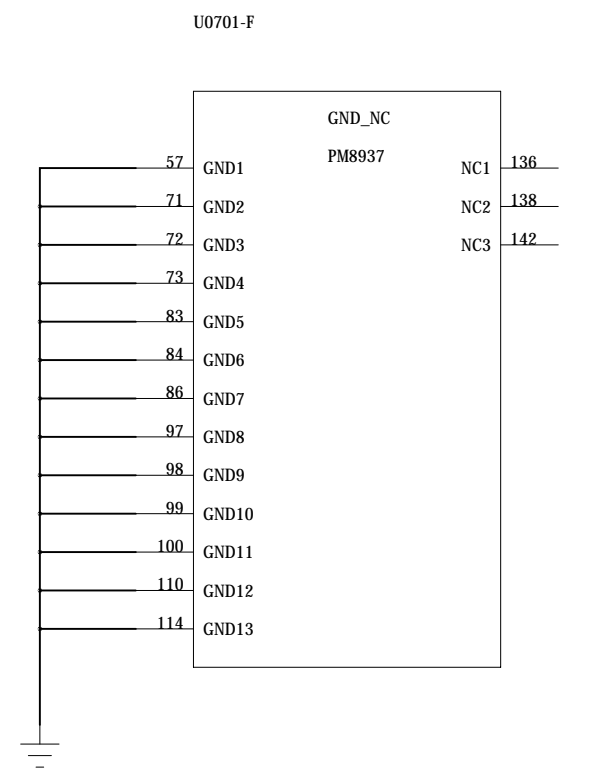


Note:
Reserve placeholder C0705 for BRCCLK signal quality
Place R0701 C0705 near PM8937

Note
GND_REF MUST connect directly to C0703 and then to main GND with a dedicated via.
GND_XO and GND_RF MUST connect directly to C0920 and C0921 respectively and then connect to main GND with dedicated via.



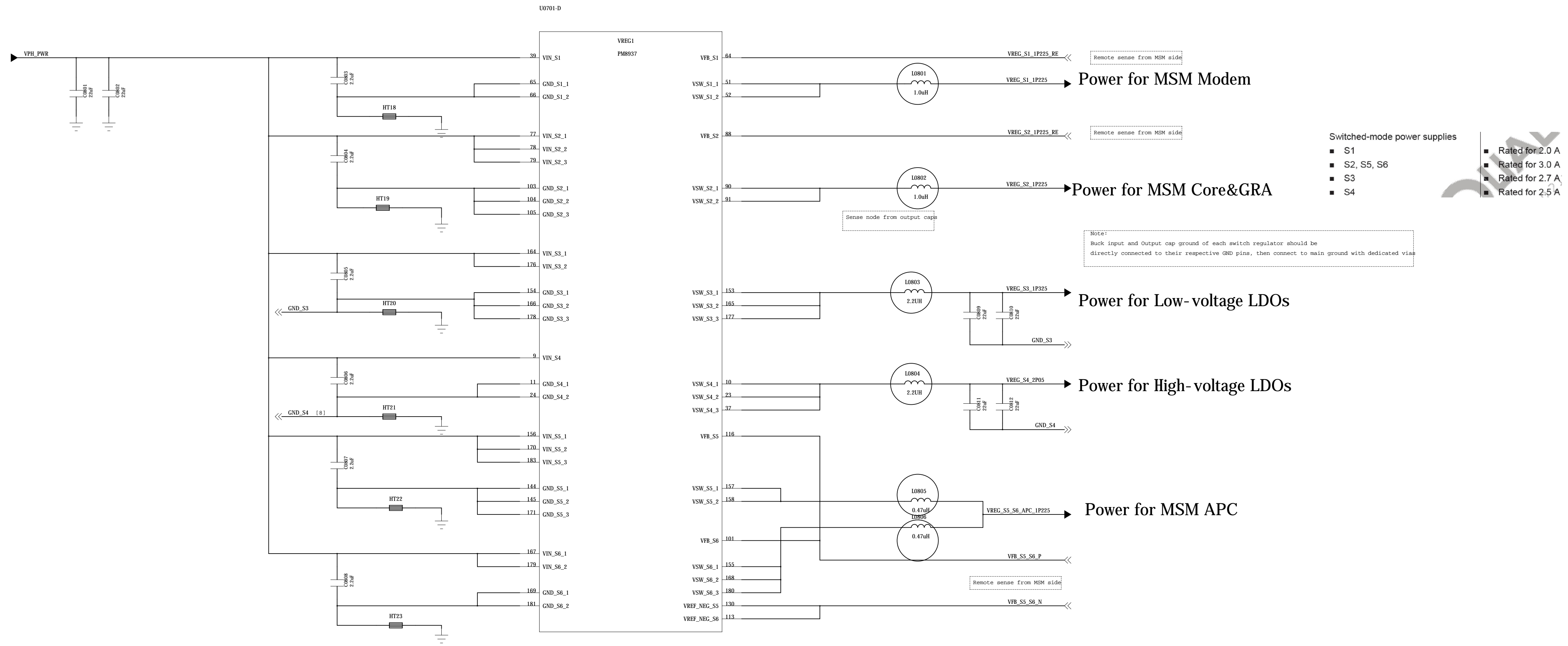
Note:
Only even MPP's can be configured as current sinks and odd MPP's as analog output buffers.



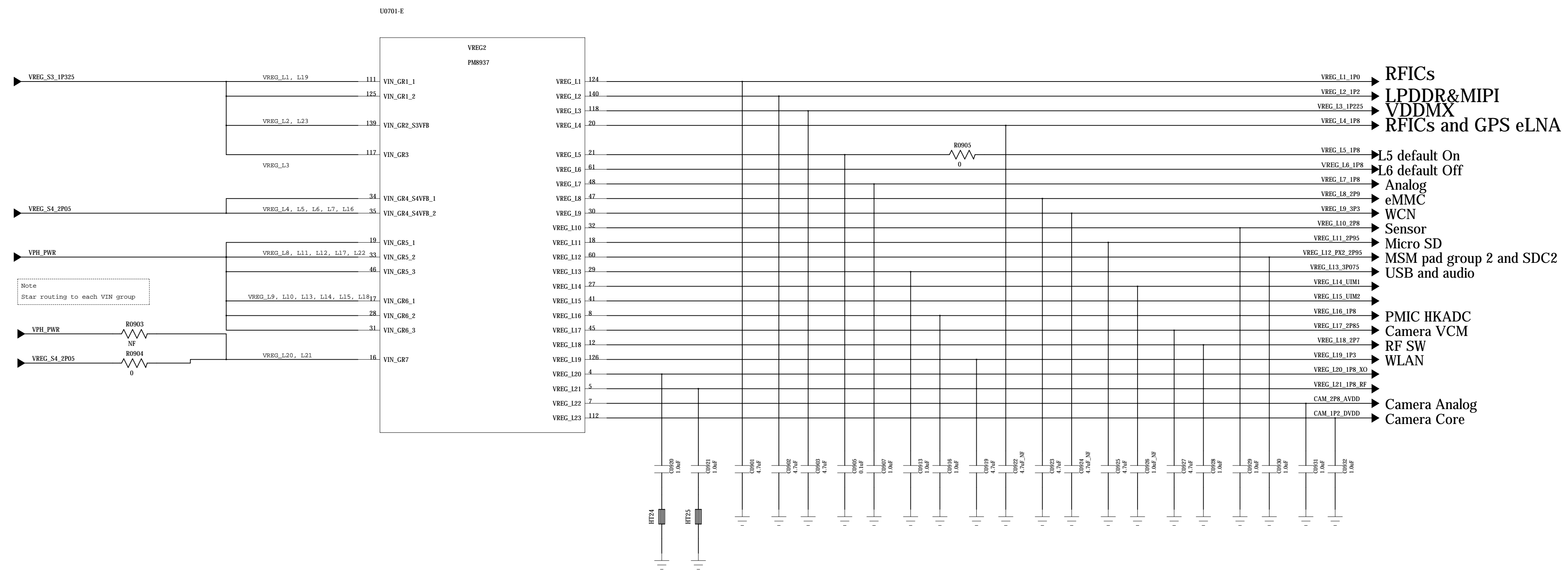
PM8937 Control and MPP/Clock



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Title Sheet _____ of _____ Size Name _____ Date: _____	

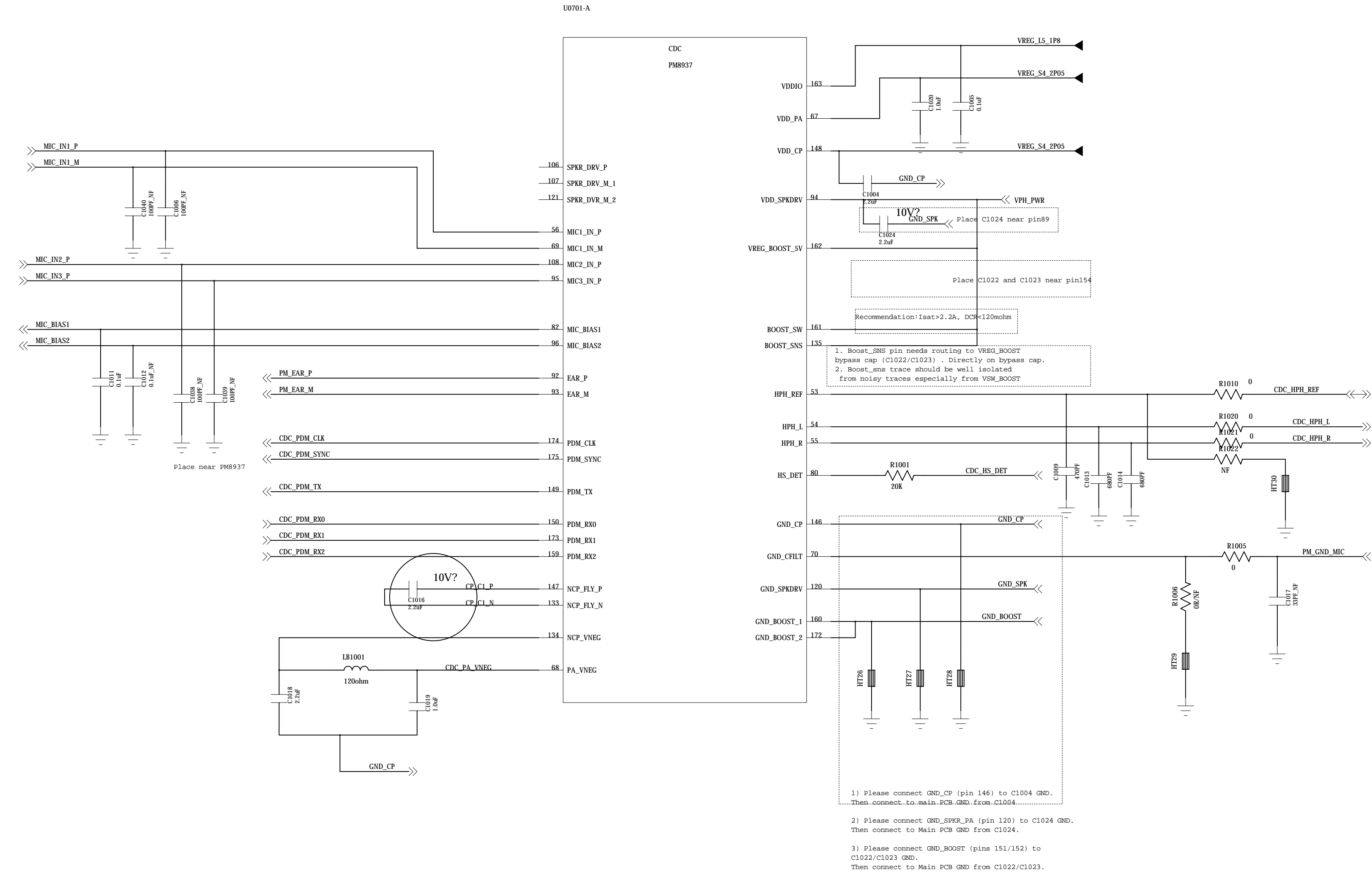


PM8937 Buck converter



PSEUDO CAPLESS LDOs
 L4*, L6, L8*, L9*, L10, L11*, L12, L14, L15, L17*, L18, L22, L23
 L4*, L8*, L9*, L11*, L17*, still need validation as Pseudo-capless
 L5, L7, L13, L16 have internal PMIC Loads and require local CAPS.

PM8937 LDO circuits

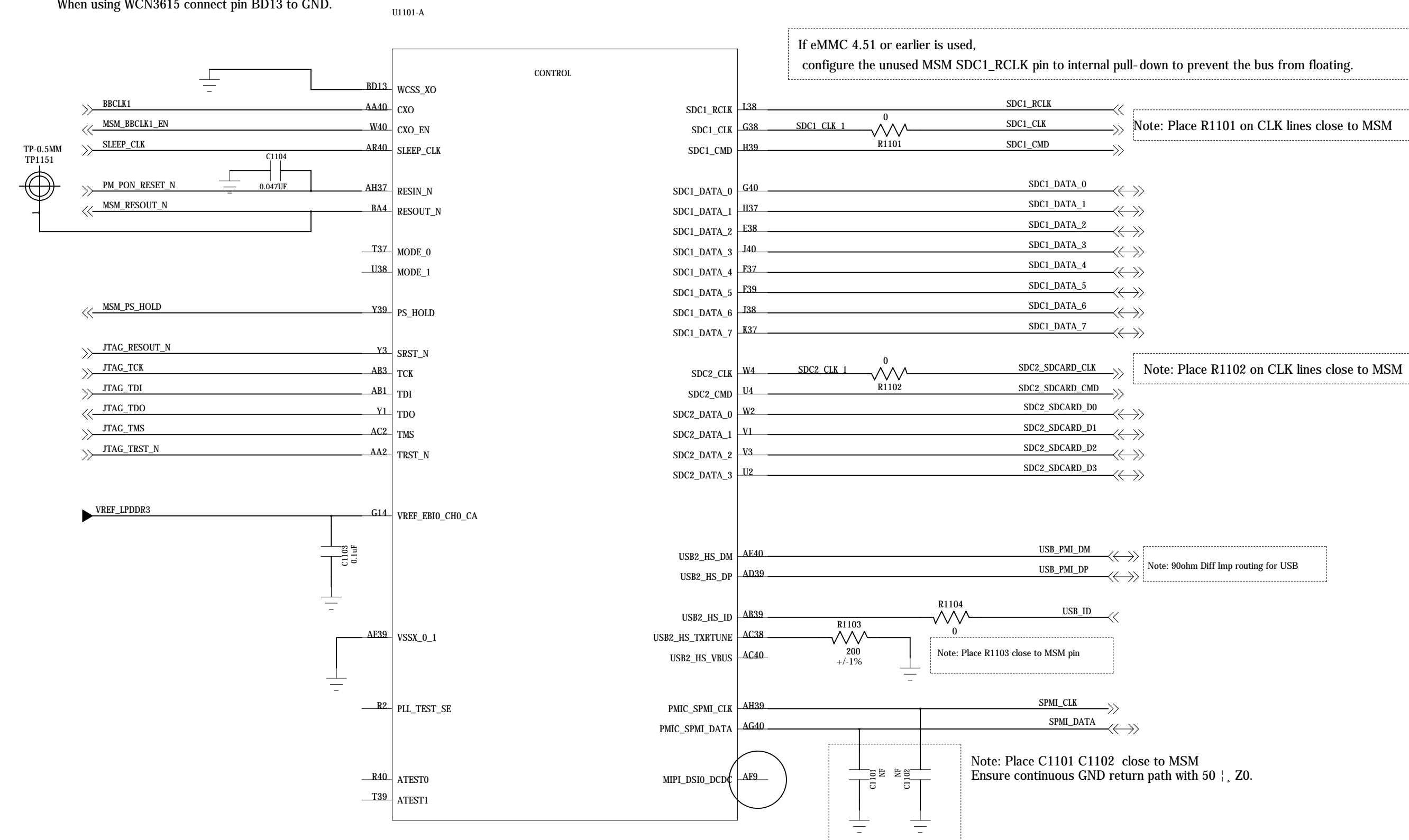


PM8937 Codec

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Note: WCSS_XO signal required only for 5CHZ.
When using WCN3615 connect pin BD13 to GND.

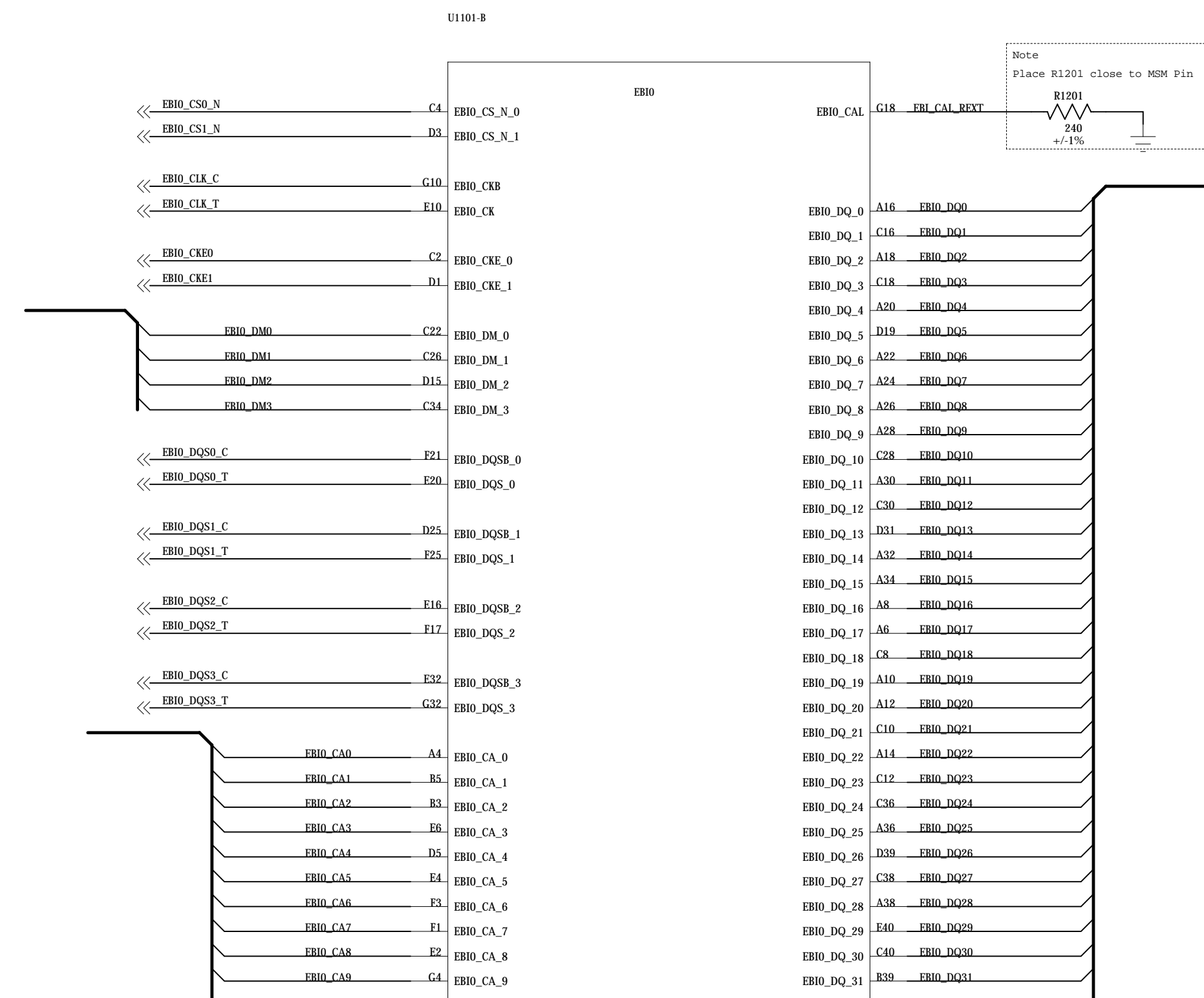


L1101 (NPL110MS) (S2) (MKT)
IND-MULTI-LAYER 2.2uH +/-20% 750MA 0603

Note:
MPI_DSIO can be configured as DCDC or LDO mode.
When configured as LDO mode, pin AF9 should be left floating and L1101 should be DNI.

DC-DC mode "C For better power ~3 mA lower

MSM8937 Control

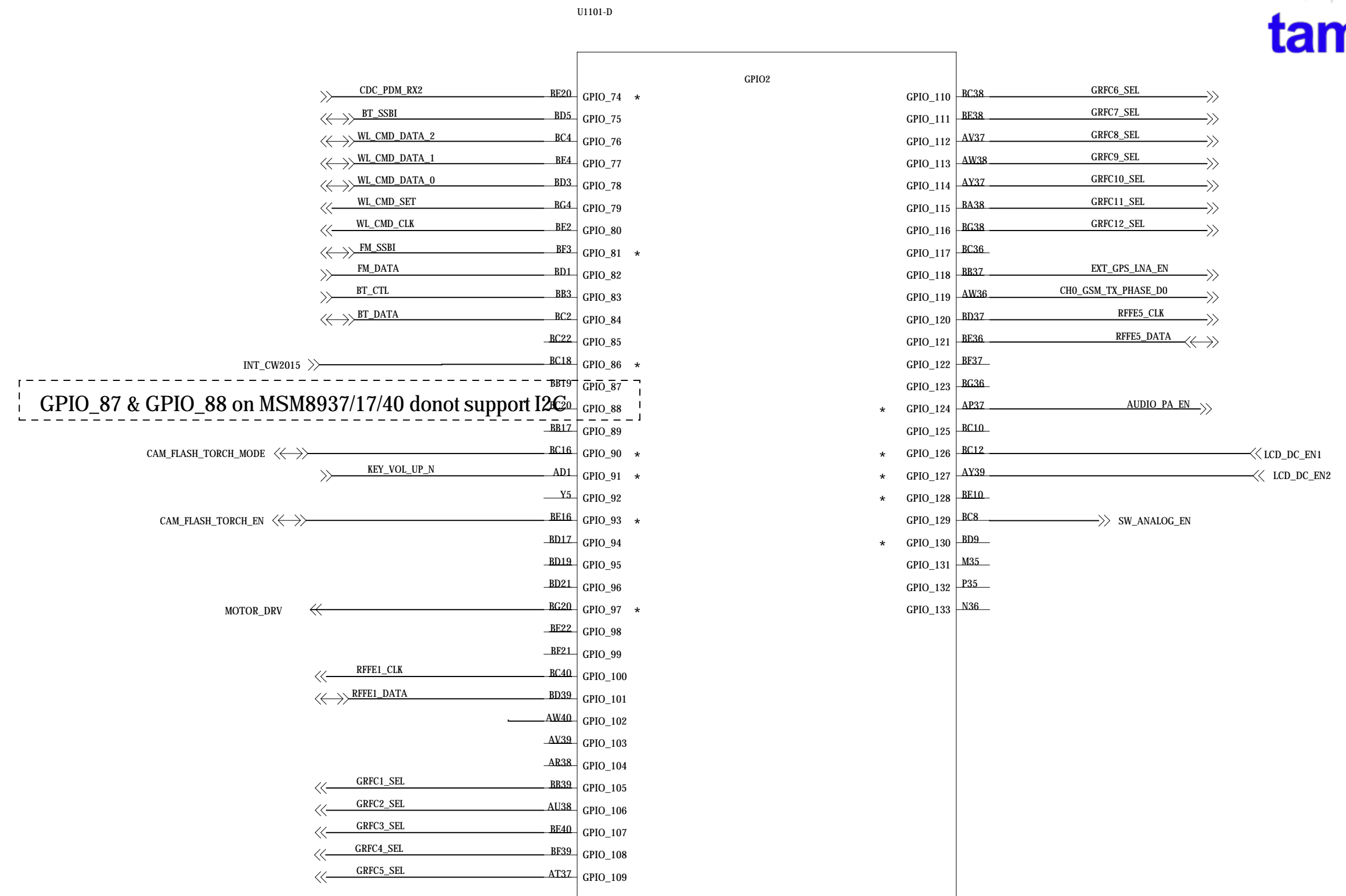
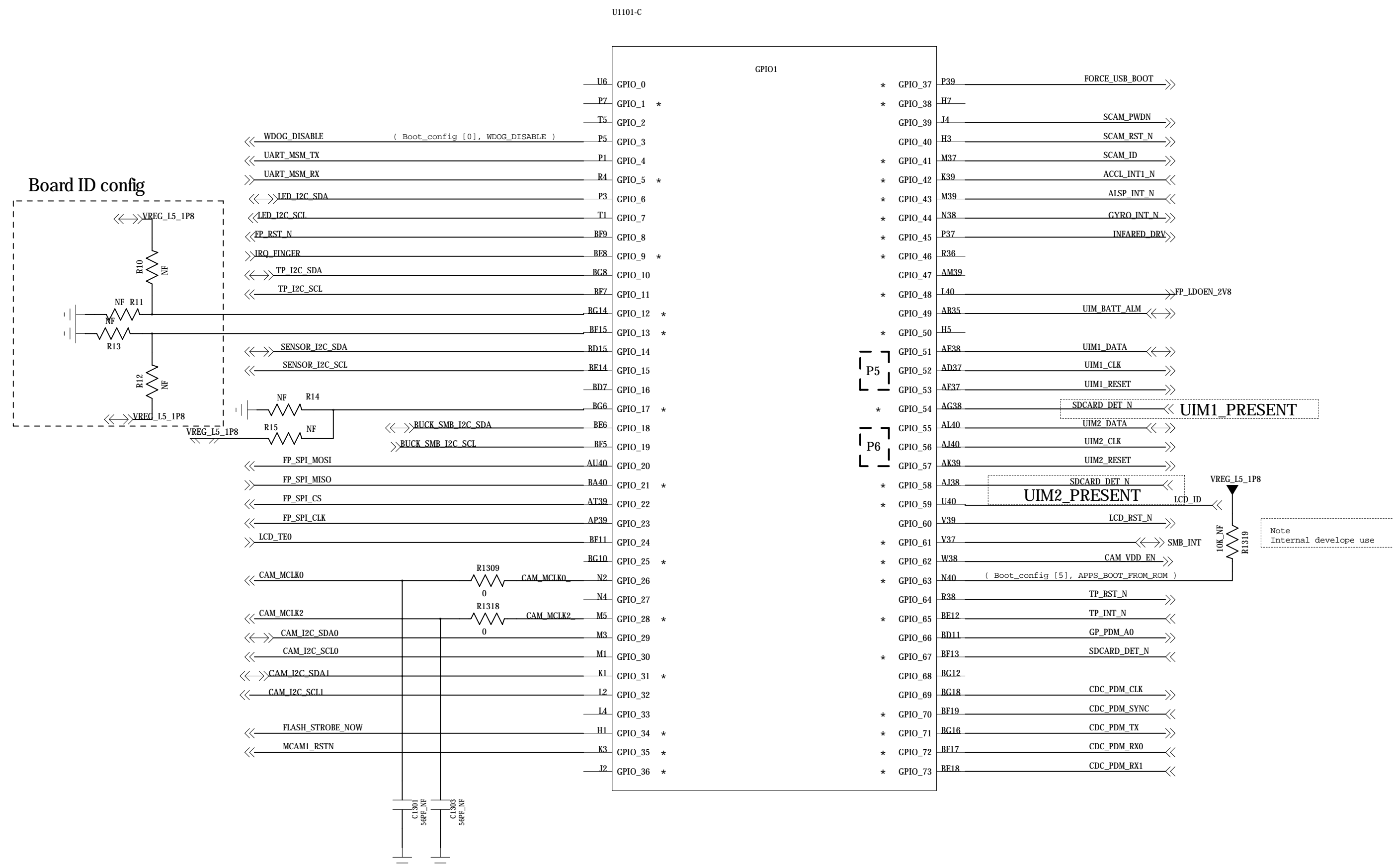


MSM8937 EBI

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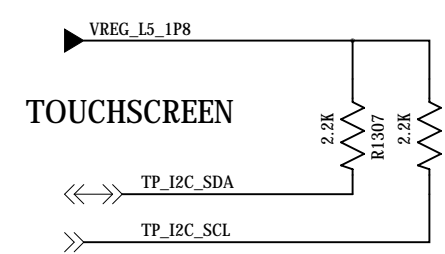
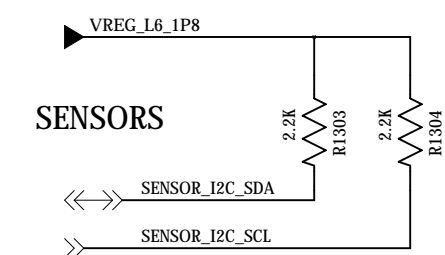
Title	
Sheet	Rev
Size	Date
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Note: Asterisks (*) indicate modem power management (MPM) wake-up pins

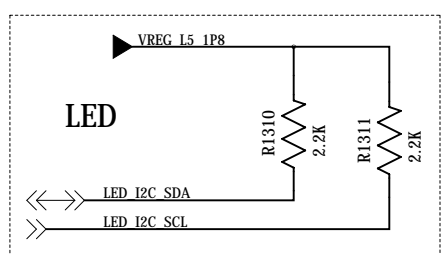
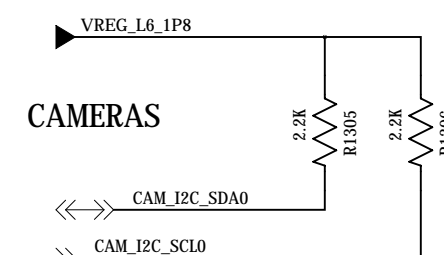


Note: Do not have pull-ups on the following GPIOs unless intend for boot or secure- boot related configurations:
GPIO_91, 107, 109

I2C PULL-UP RESISTORS



Note: Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.



GPIO	BOOT_CONFIG
GPIO_3	BOOT_CONFIG[0]/WDOG_DISABLE
GPIO_111	BOOT_CONFIG[1]
GPIO_112	BOOT_CONFIG[2]
GPIO_88	BOOT_CONFIG[3]

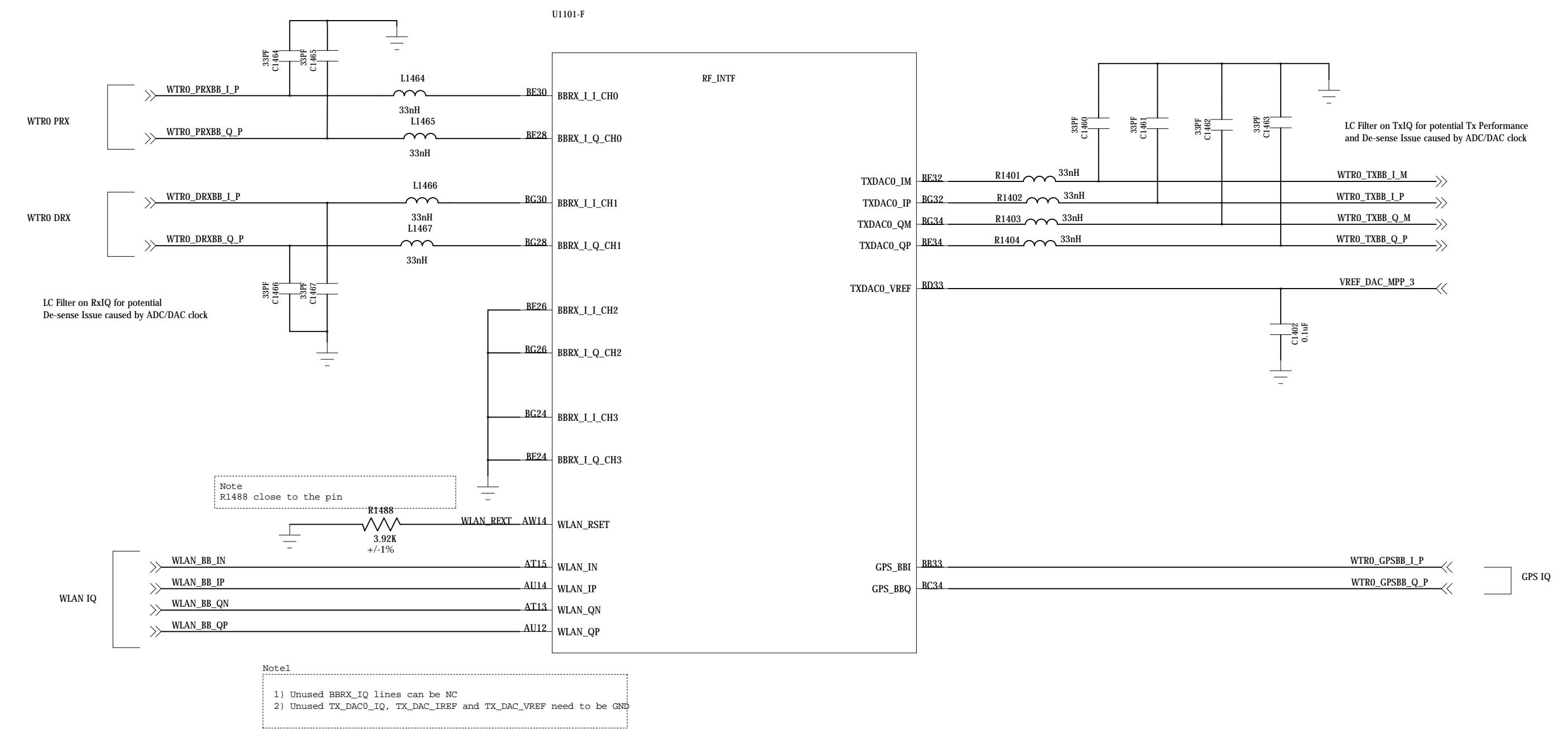
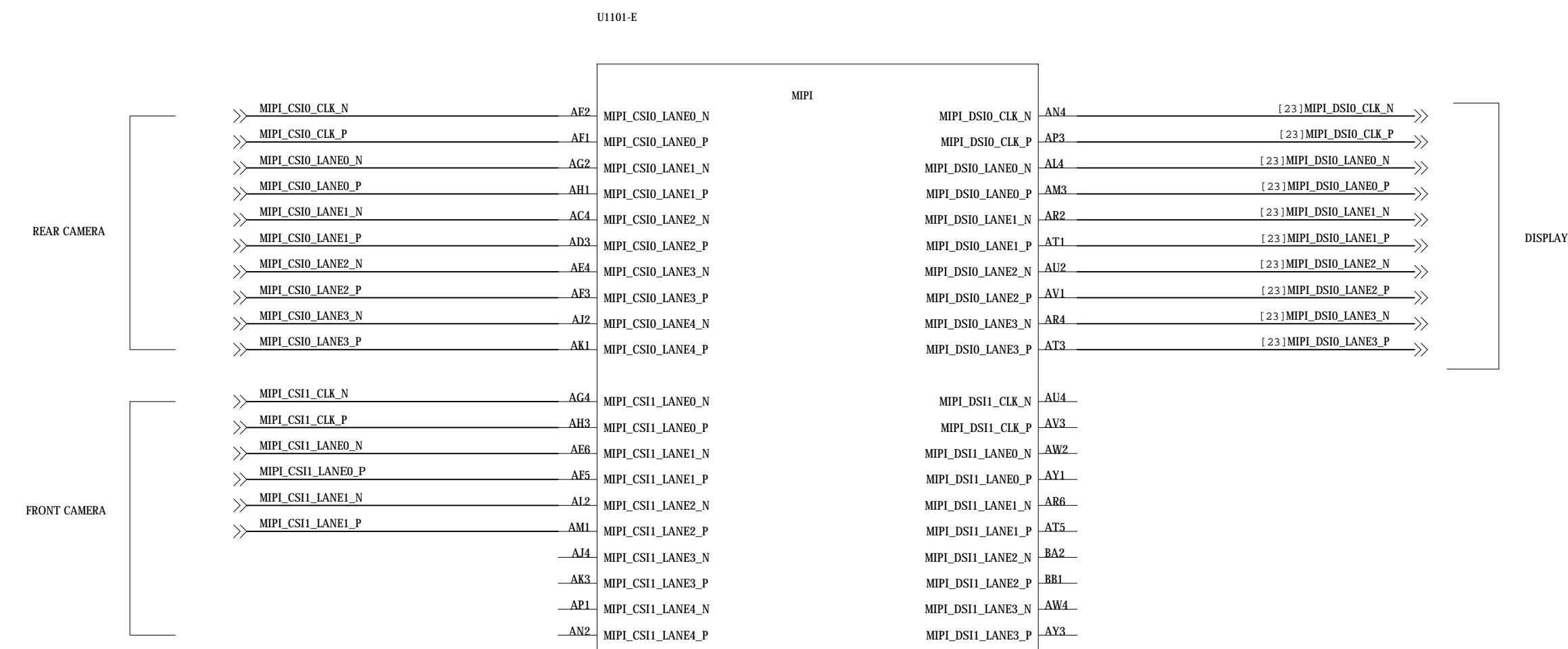
BOOT_CONFIG[3:1]	BOOT_CONFIG
0b000	SDC1 -> SDC2 -> USB2.0
0b010	SDC1
0b100	SDC2-> SDC1

Default Boot Config (0b000) is SDC1(0b0C)

MSM8937 GPIO

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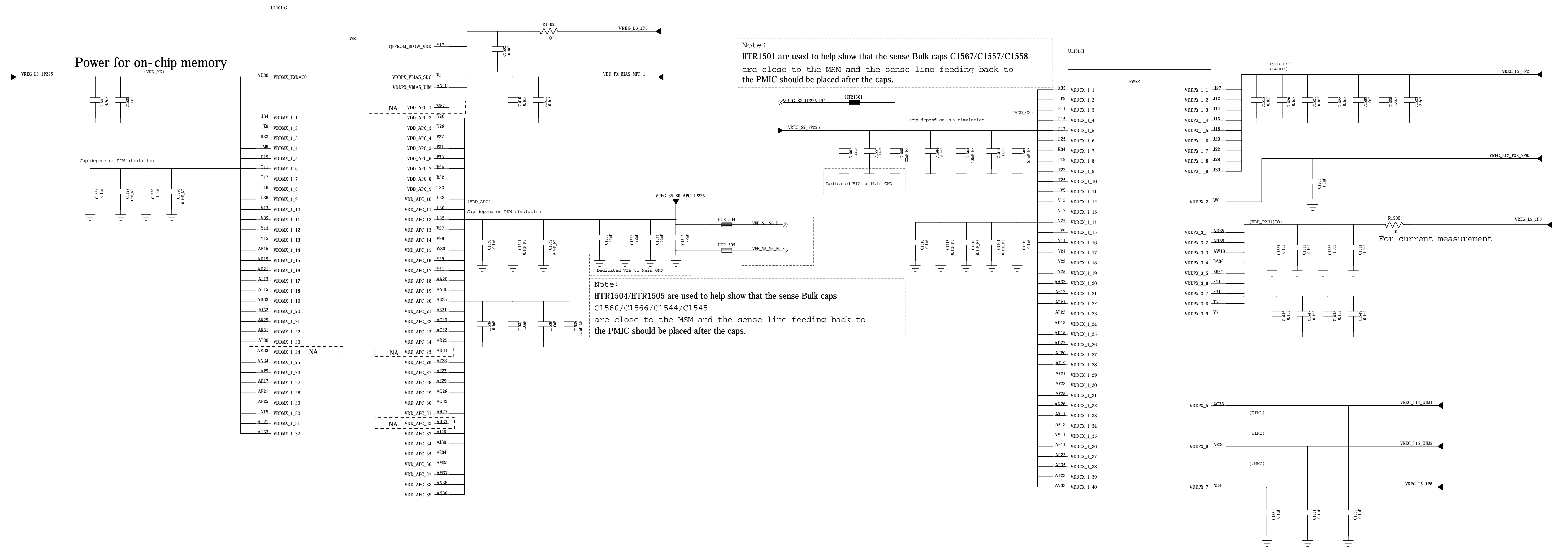


Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

MSM8937 MIPI and RF Control



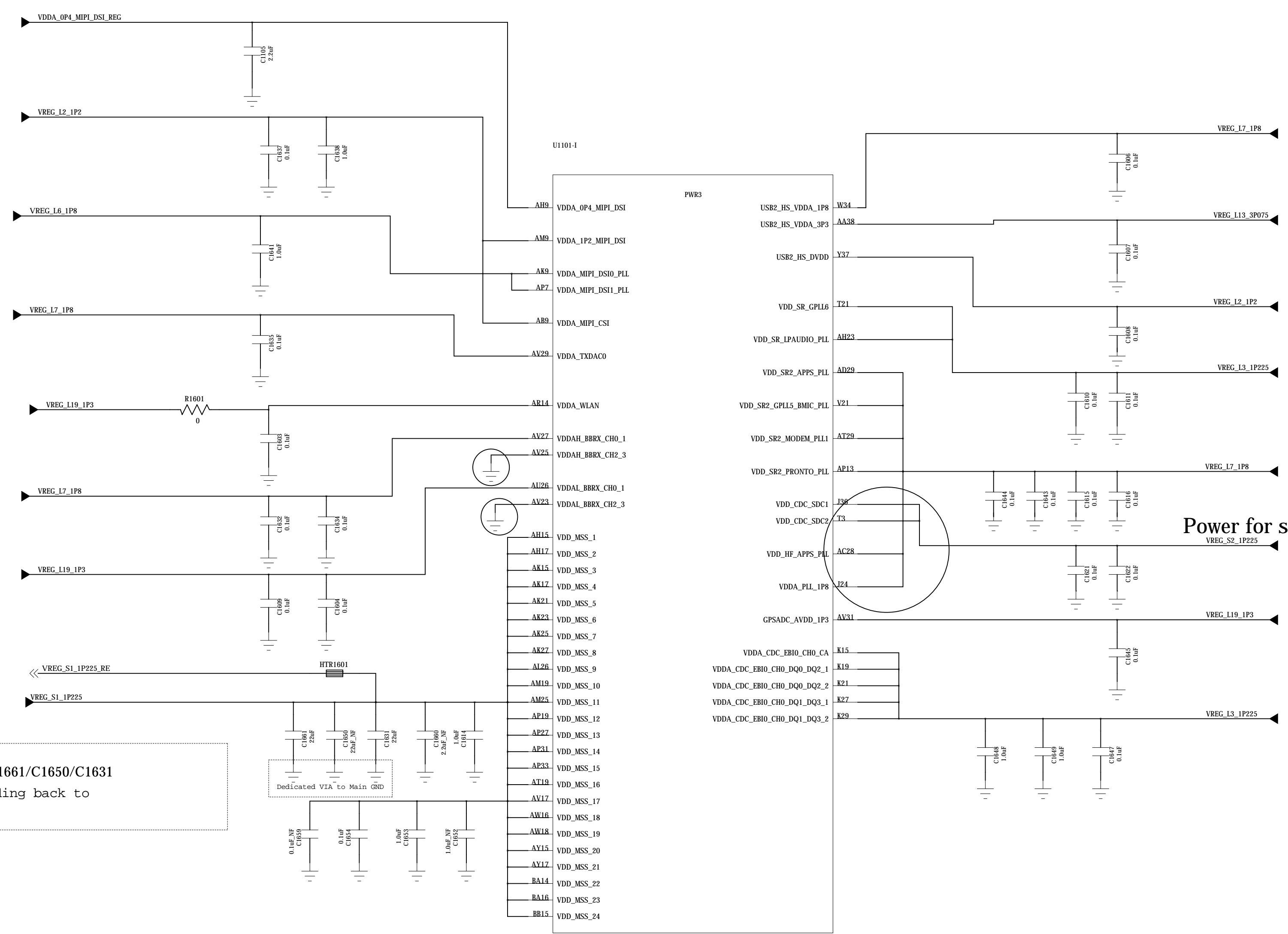
tamiraat.com منبع مقاله



MSM8937 POWER1

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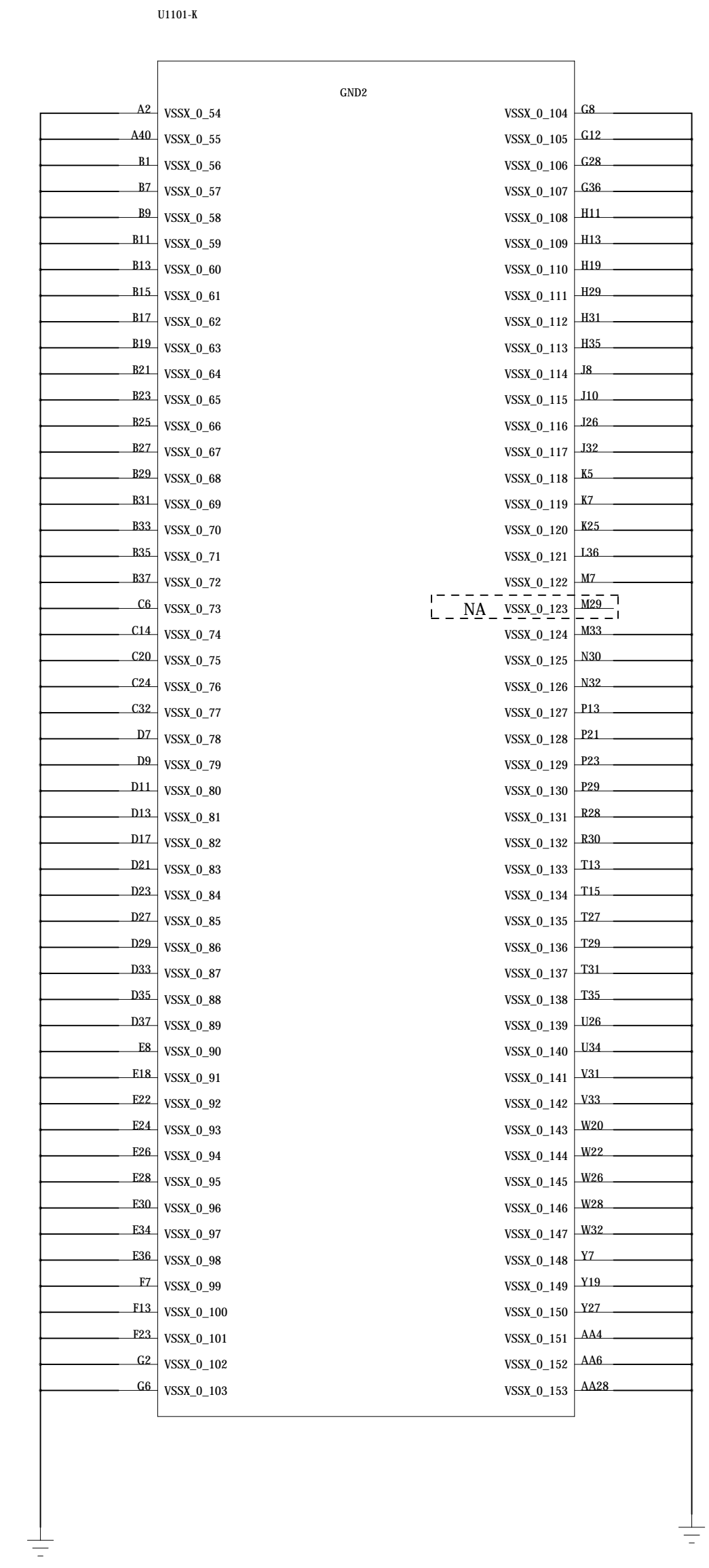
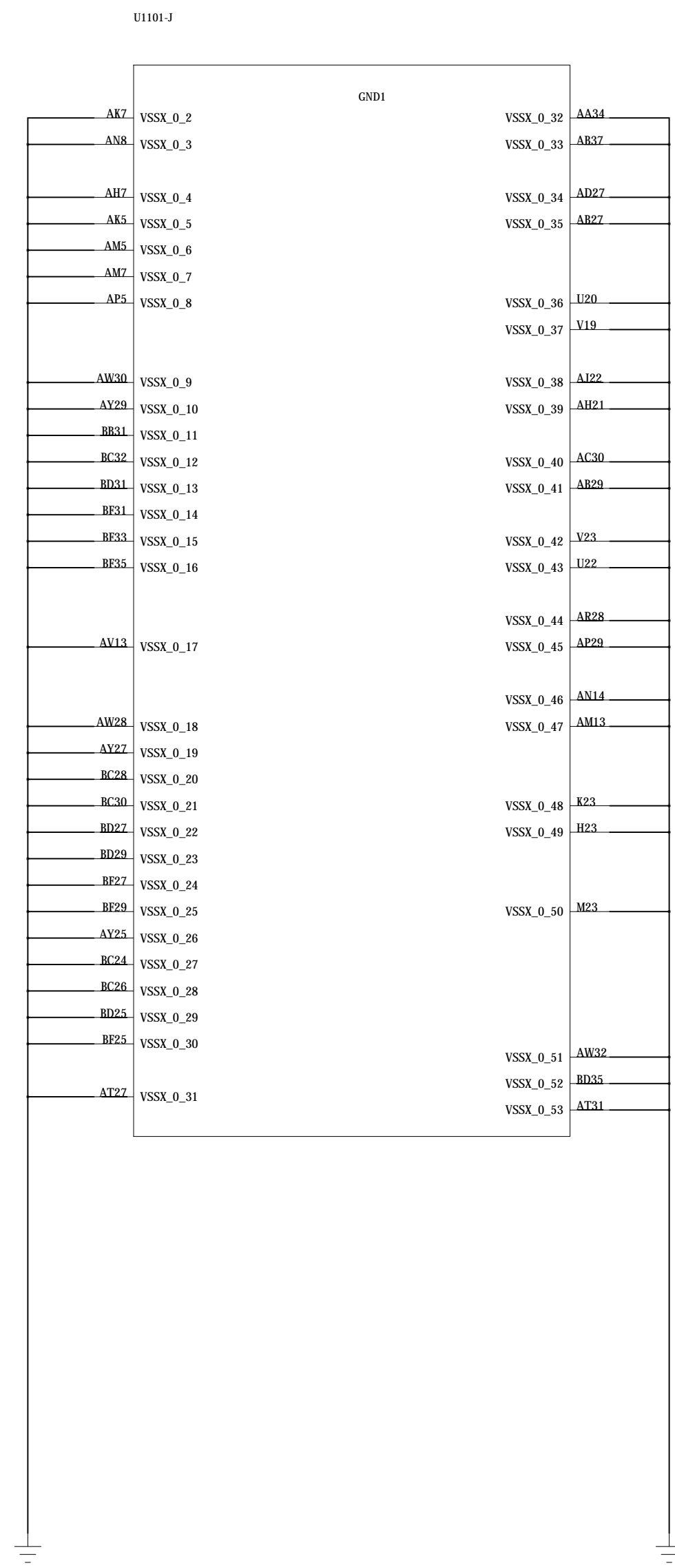
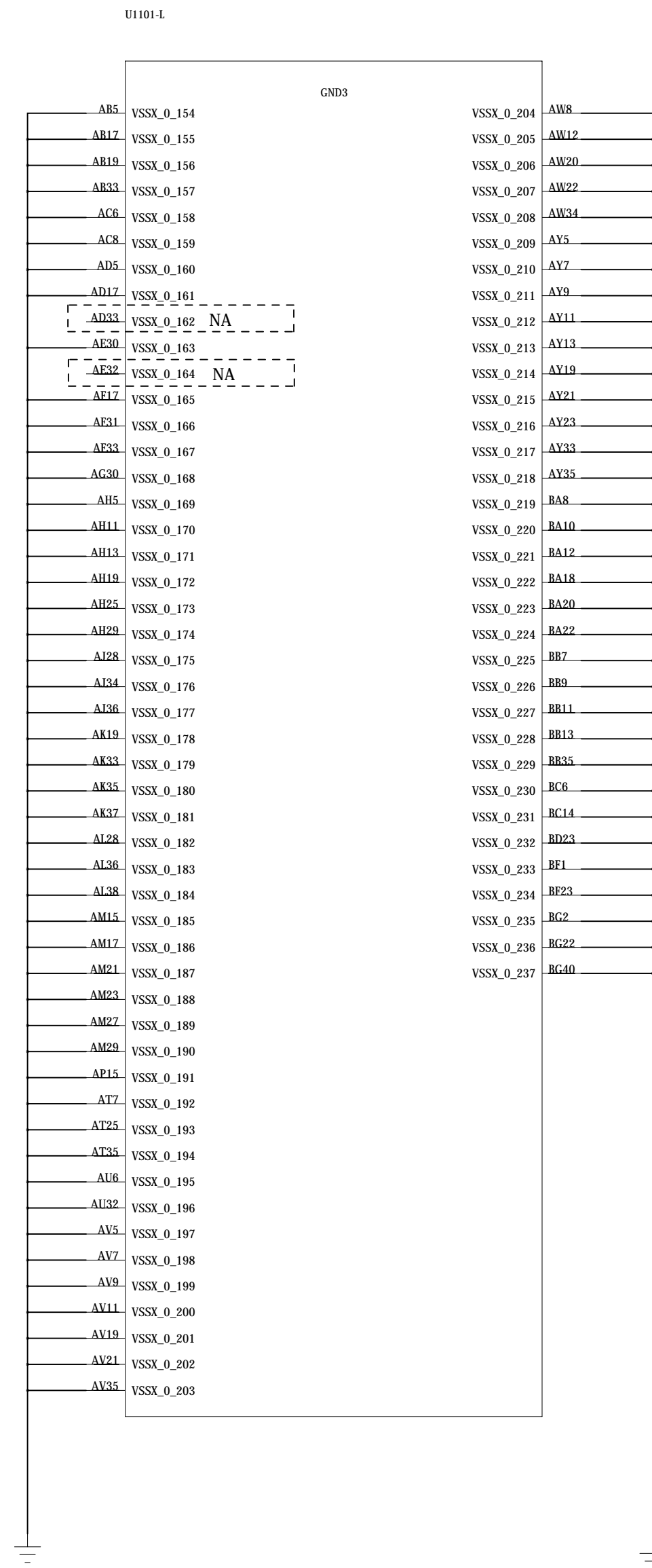
Title	
Sheet	Rev
Date:	Sheet of



Note:
HTR1601 are used to help show that the sense Bulk caps C1661/C1650/C1631 are close to the MSM and the sense line feeding back to the PMIC should be placed after the caps.

Power for secure digital calibration delay circuits

MSM8937 POWER2

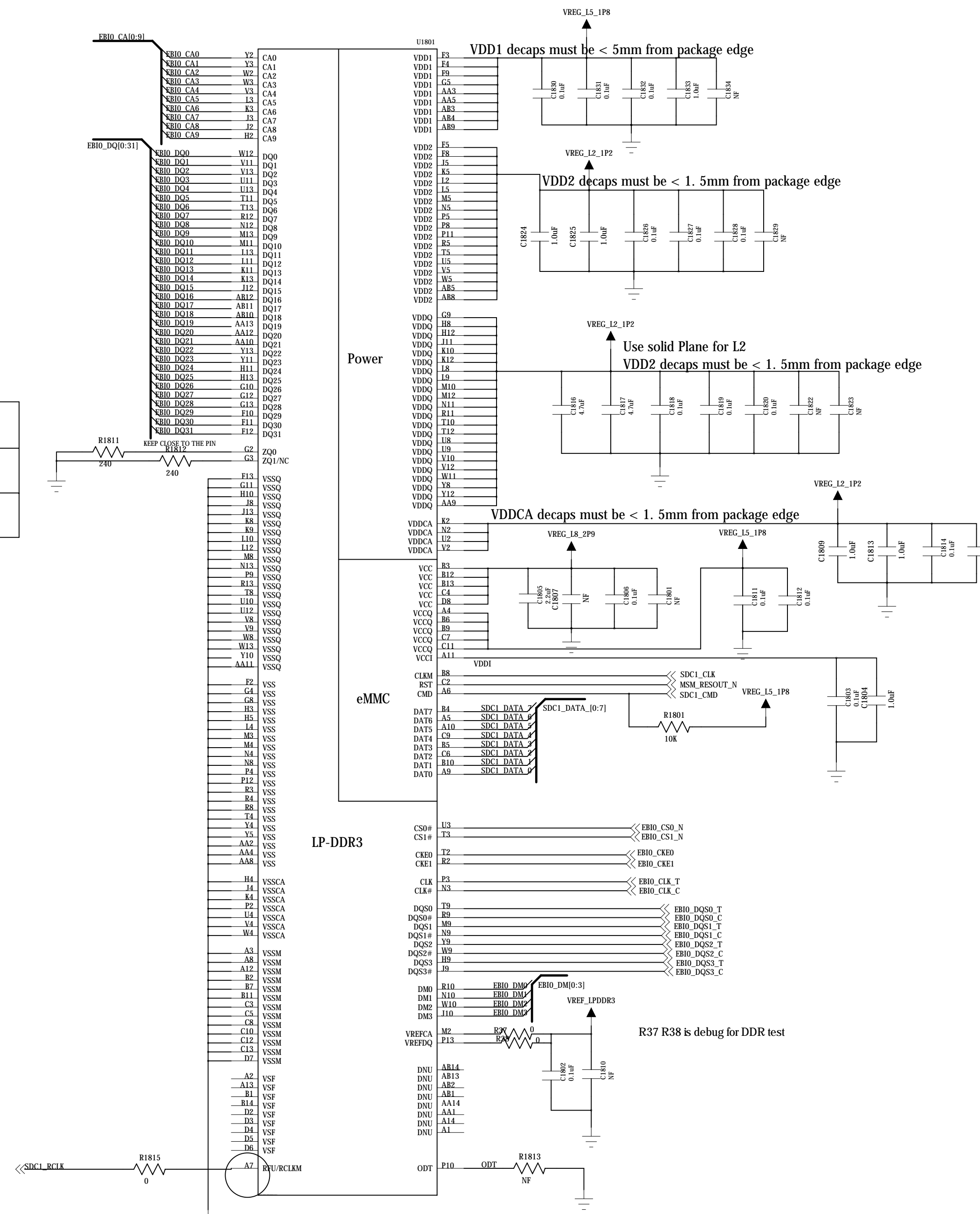


MSM8937 GND

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Title	
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Size	Name
Date:	Sheet of

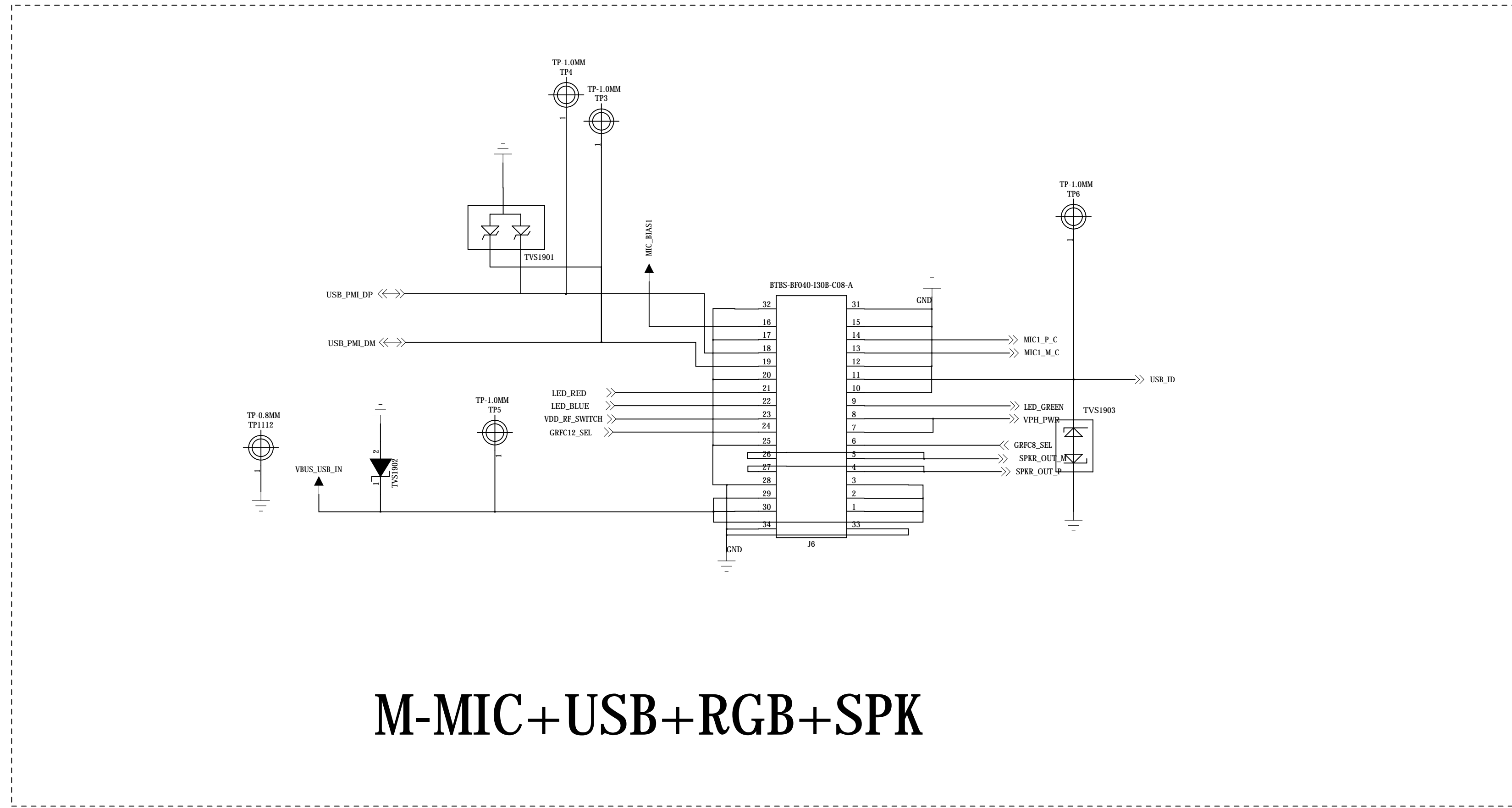
	MICRO/HYNIX	SAMSUNG
U1501.G3	ZQ1	NC
U1501.A7	RFU	RCLK



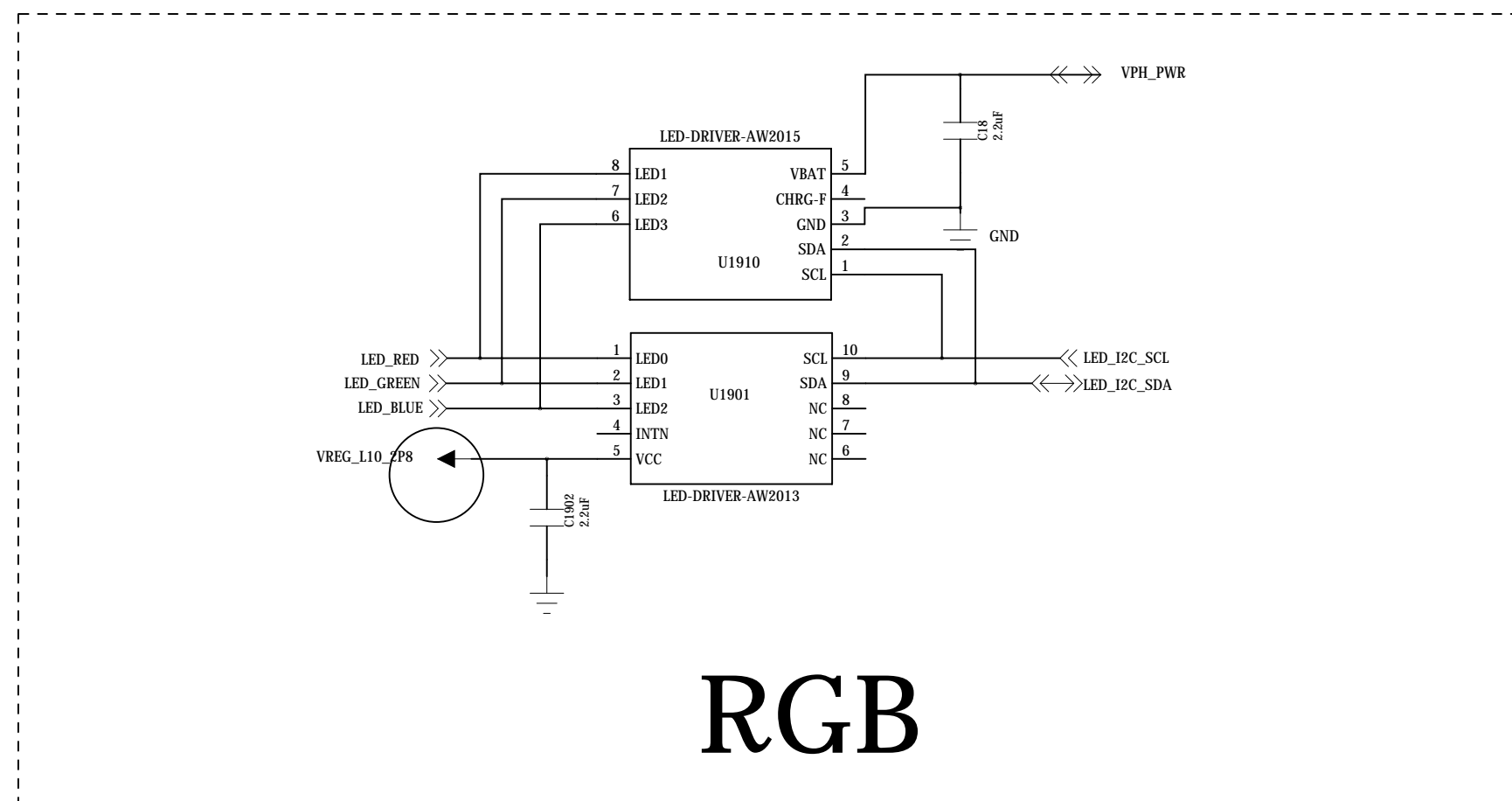
MEMORY:LPDDR3+EMMC

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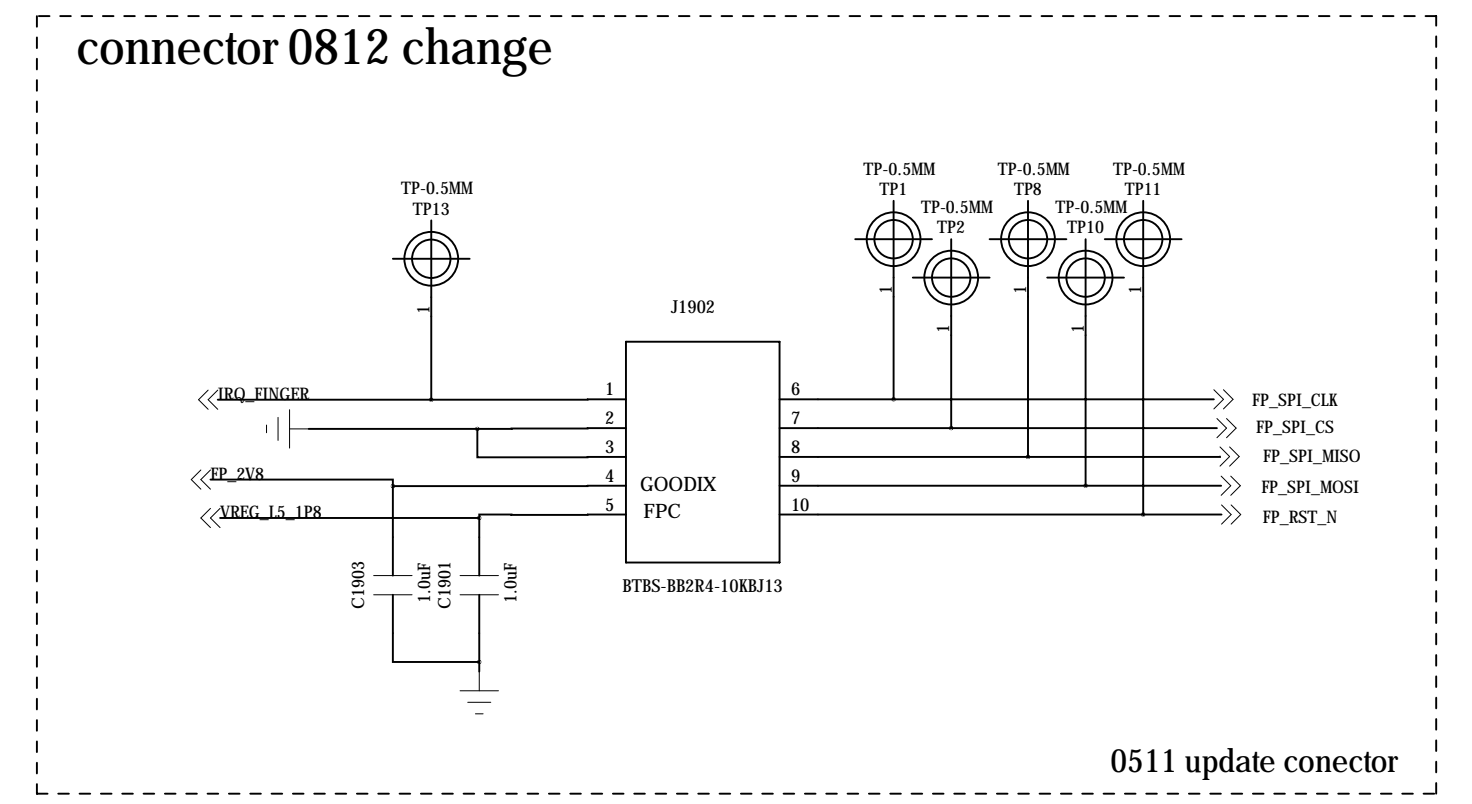
M-MIC+USB+RGB+SPK



RGB

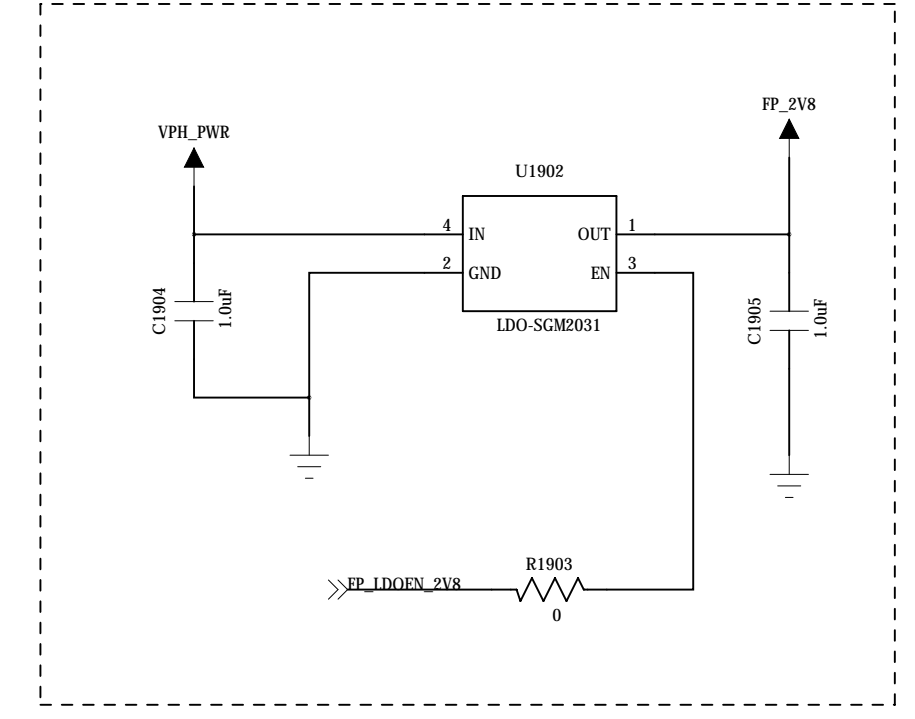
I2C Address	
Write	8B0x8A
Read	8B0x8B

Power on sequence: can be applied in any order

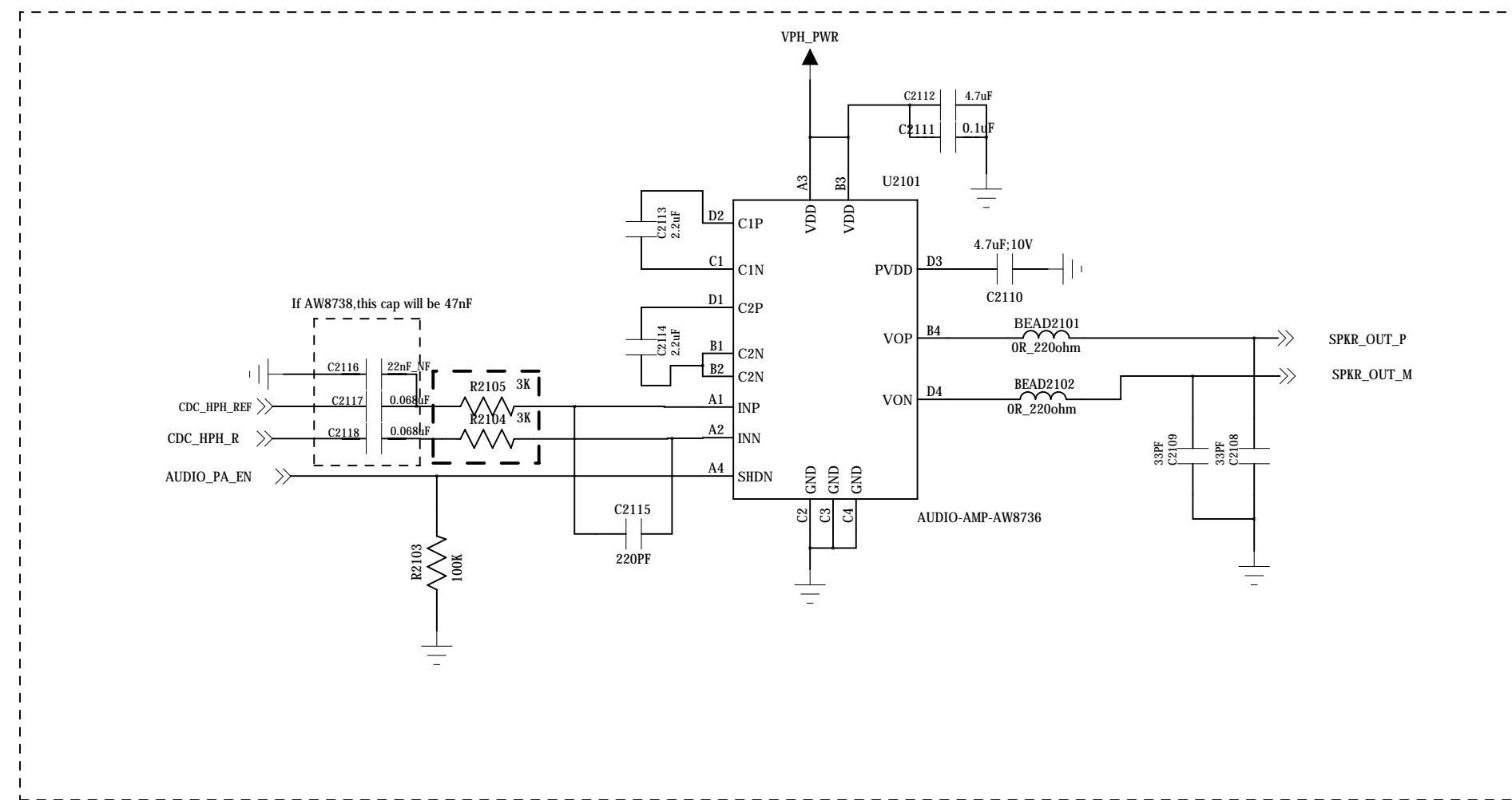


connector 0812 change

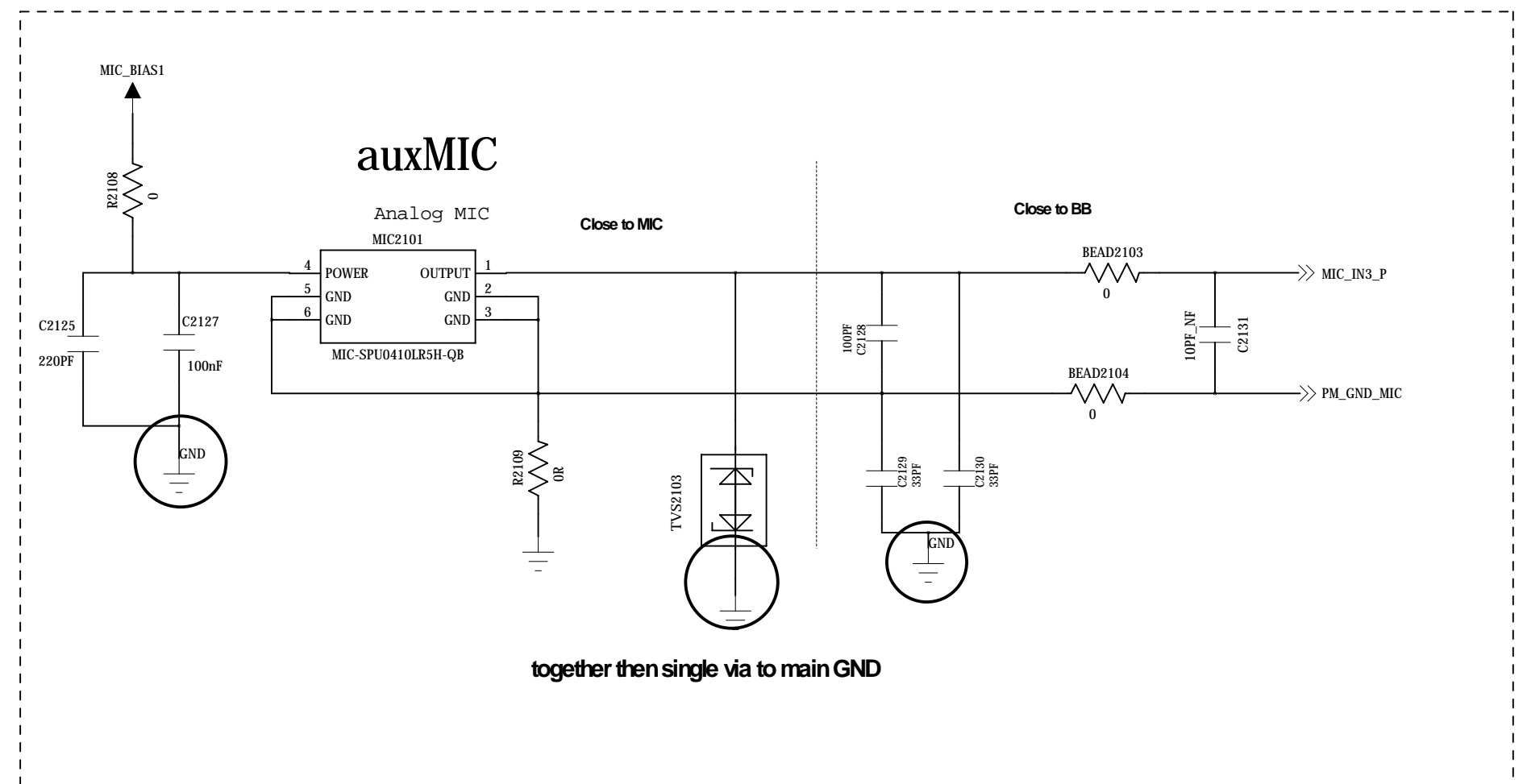
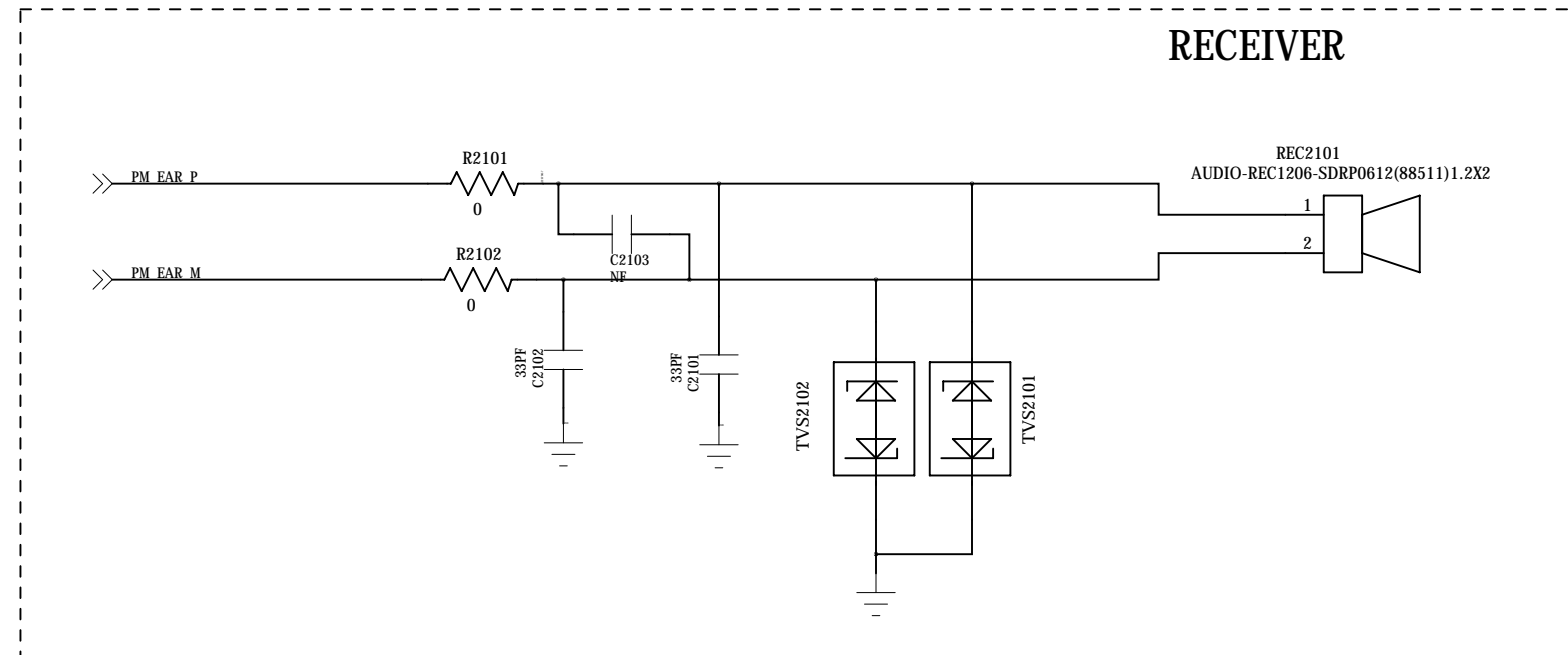
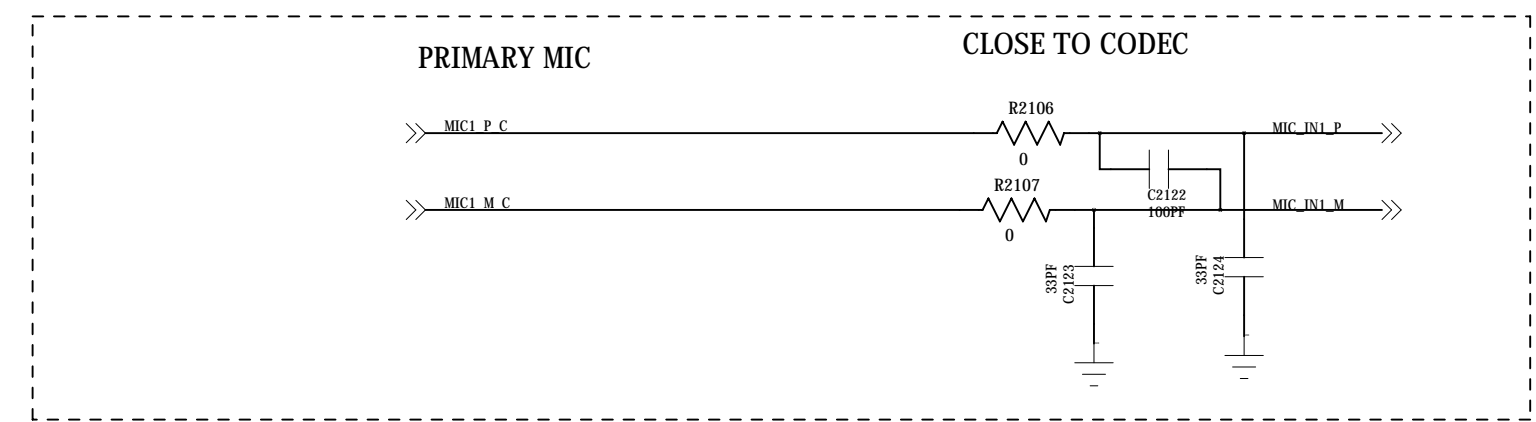
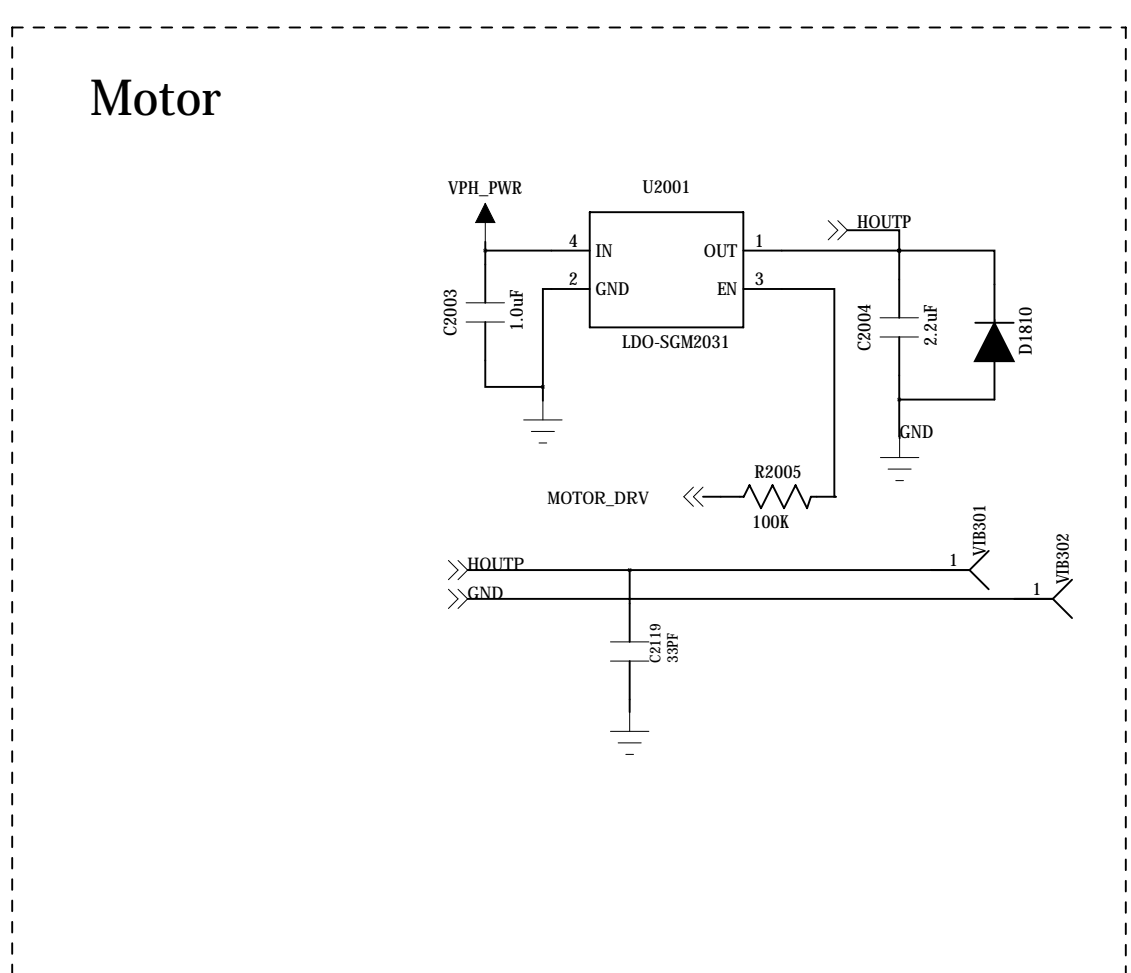
0511 update conector



USB/SUB BOARD CONNECTOR

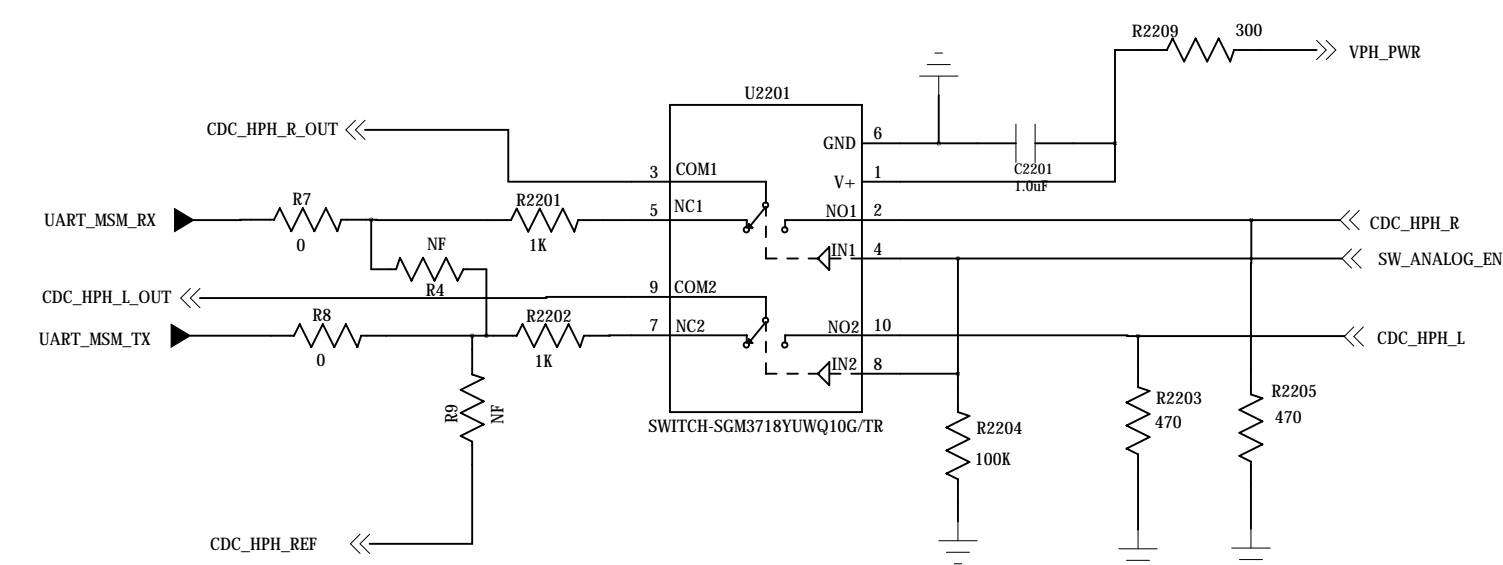
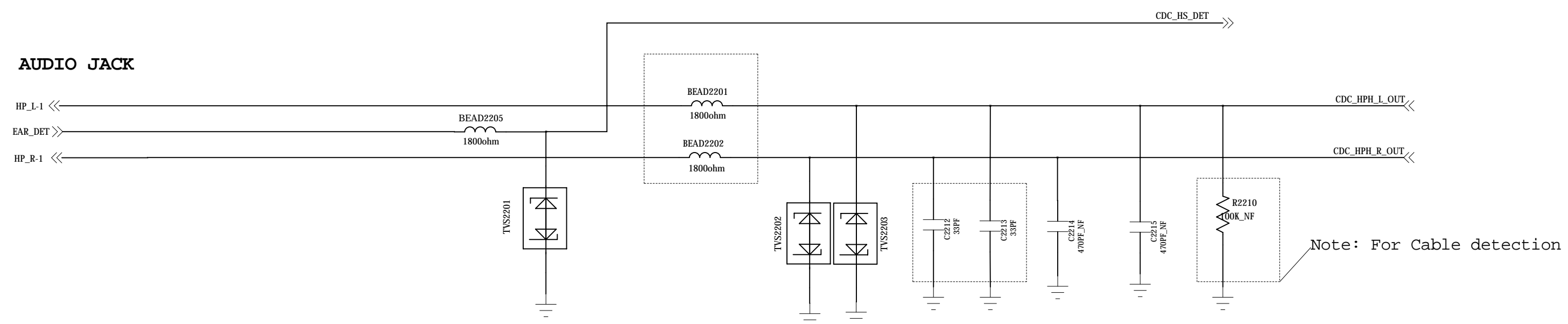
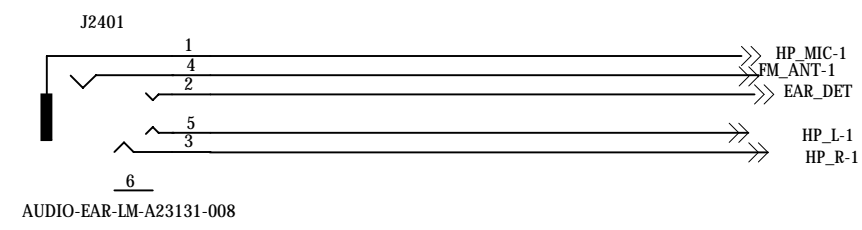


close to SPK

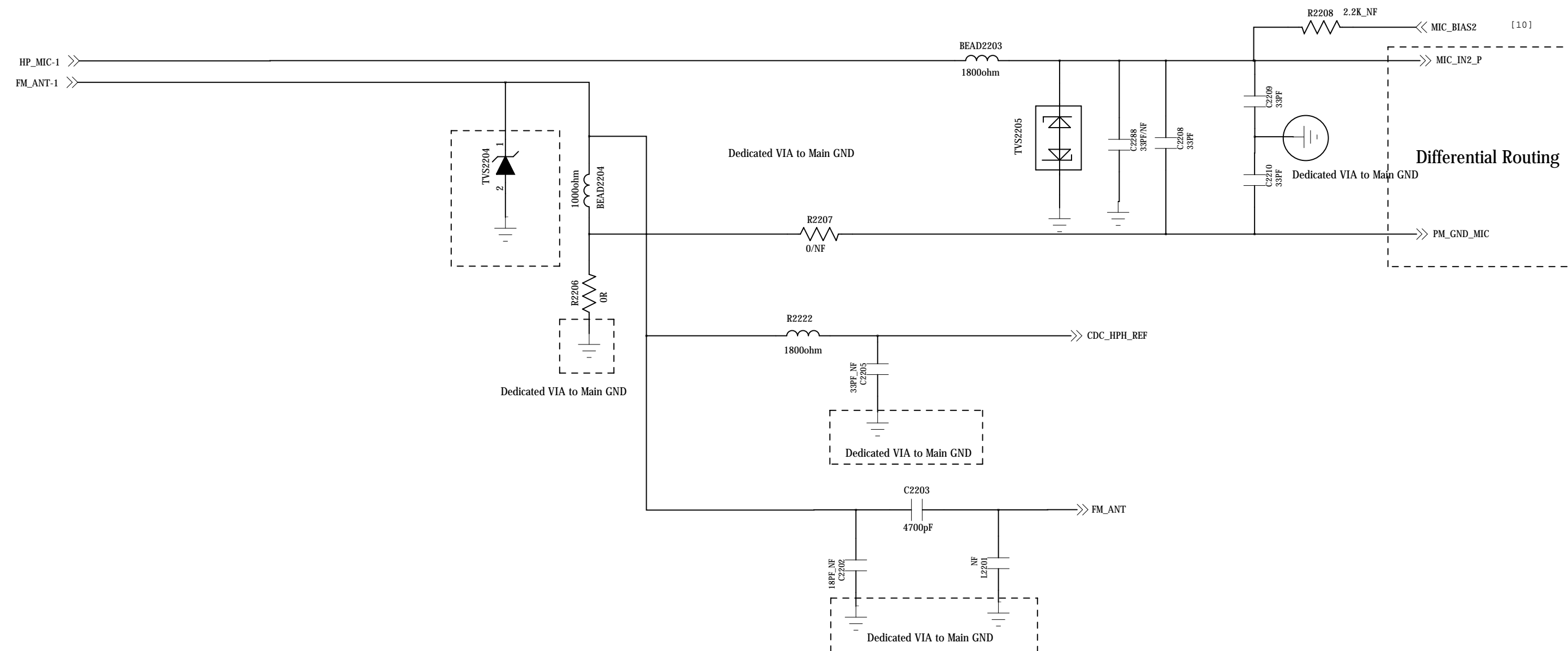


SECONDARY MIC/RECEIVER

Note: Ferrite beads and their corresponding bypass capacitors on CDC_HPH_L, CDC_HPH_R and CDC_HPH_REF are needed to reduce noise generated by audio/FM concurrency



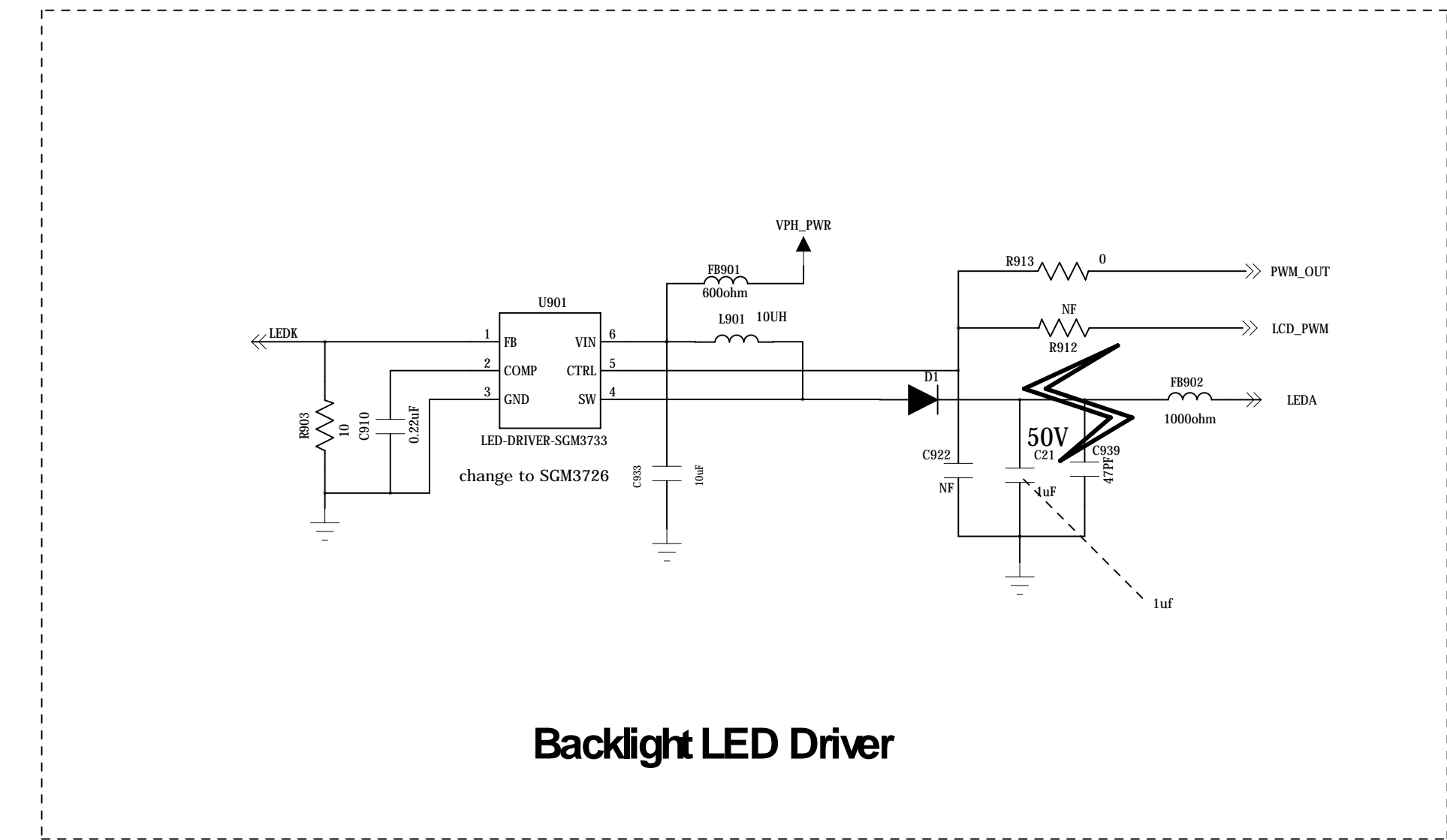
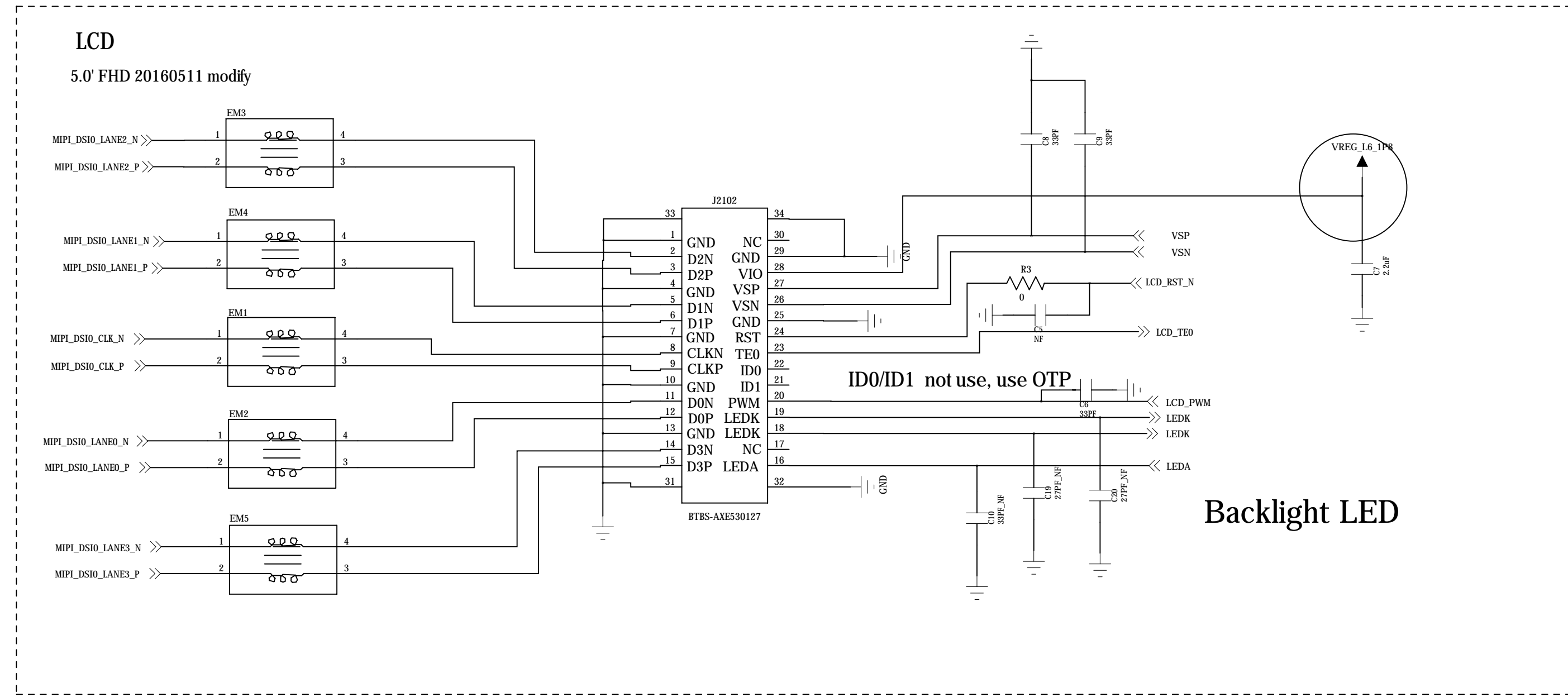
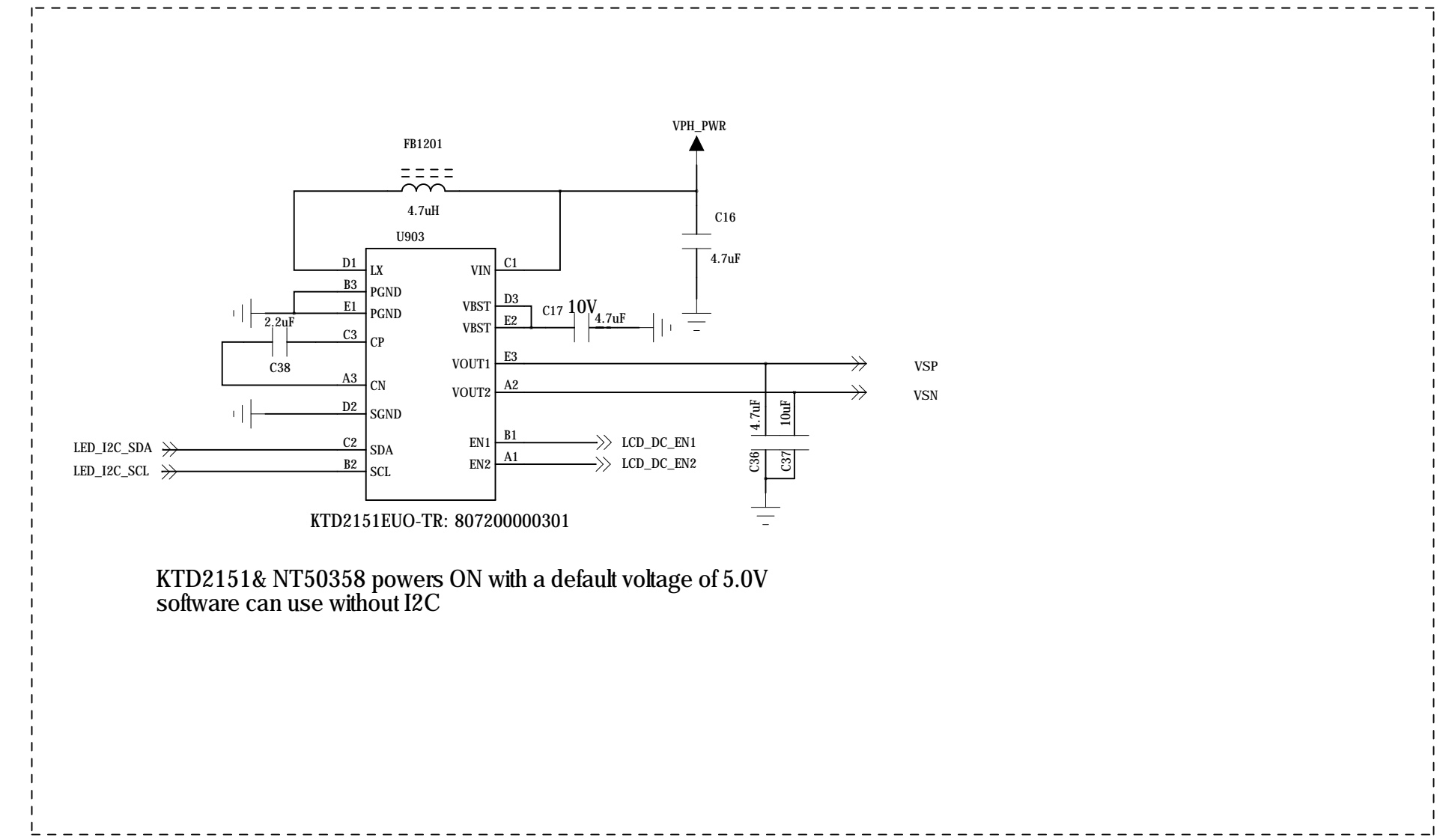
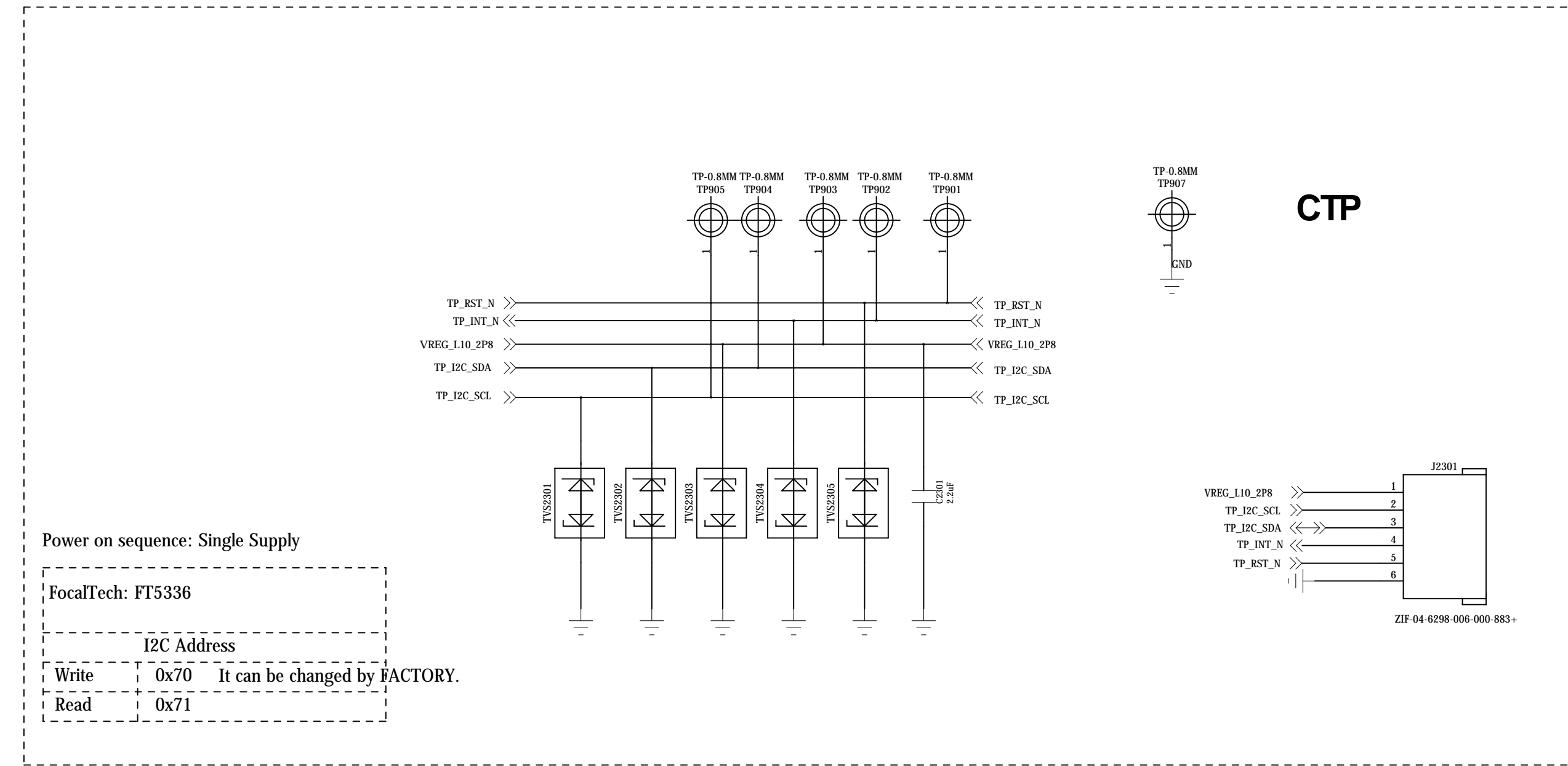
IN=0, COM Connected to NC;
IN=1, COM Connected to NO;



EARPHONE

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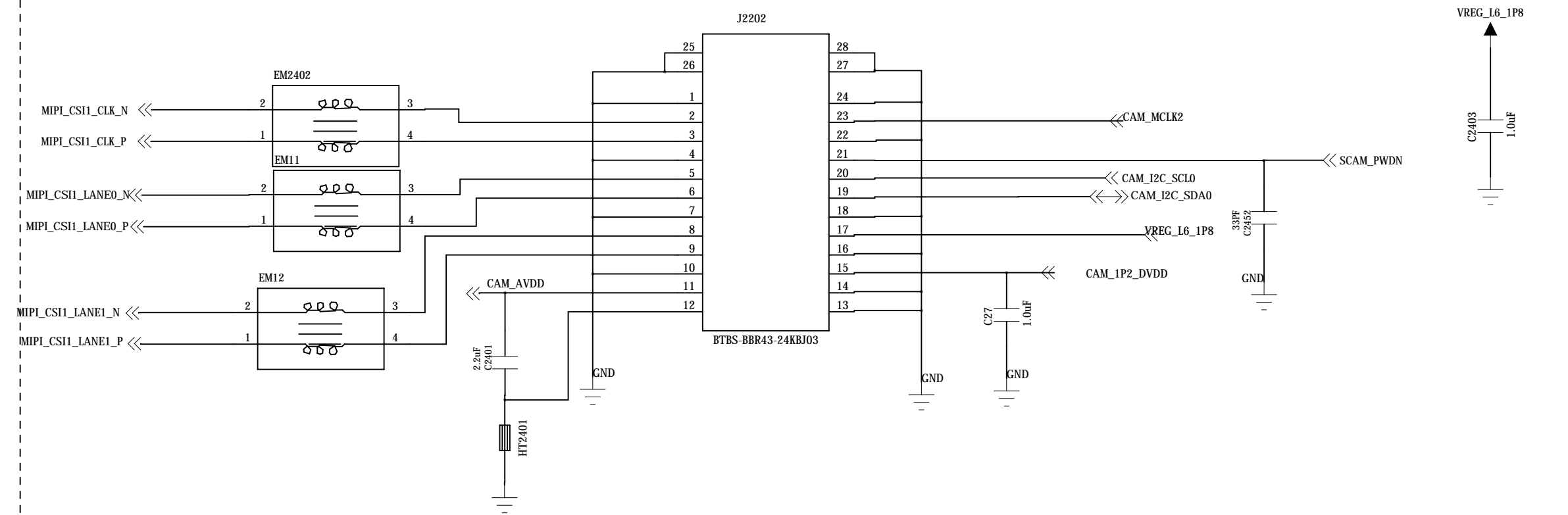
Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

LCD interface and backlight

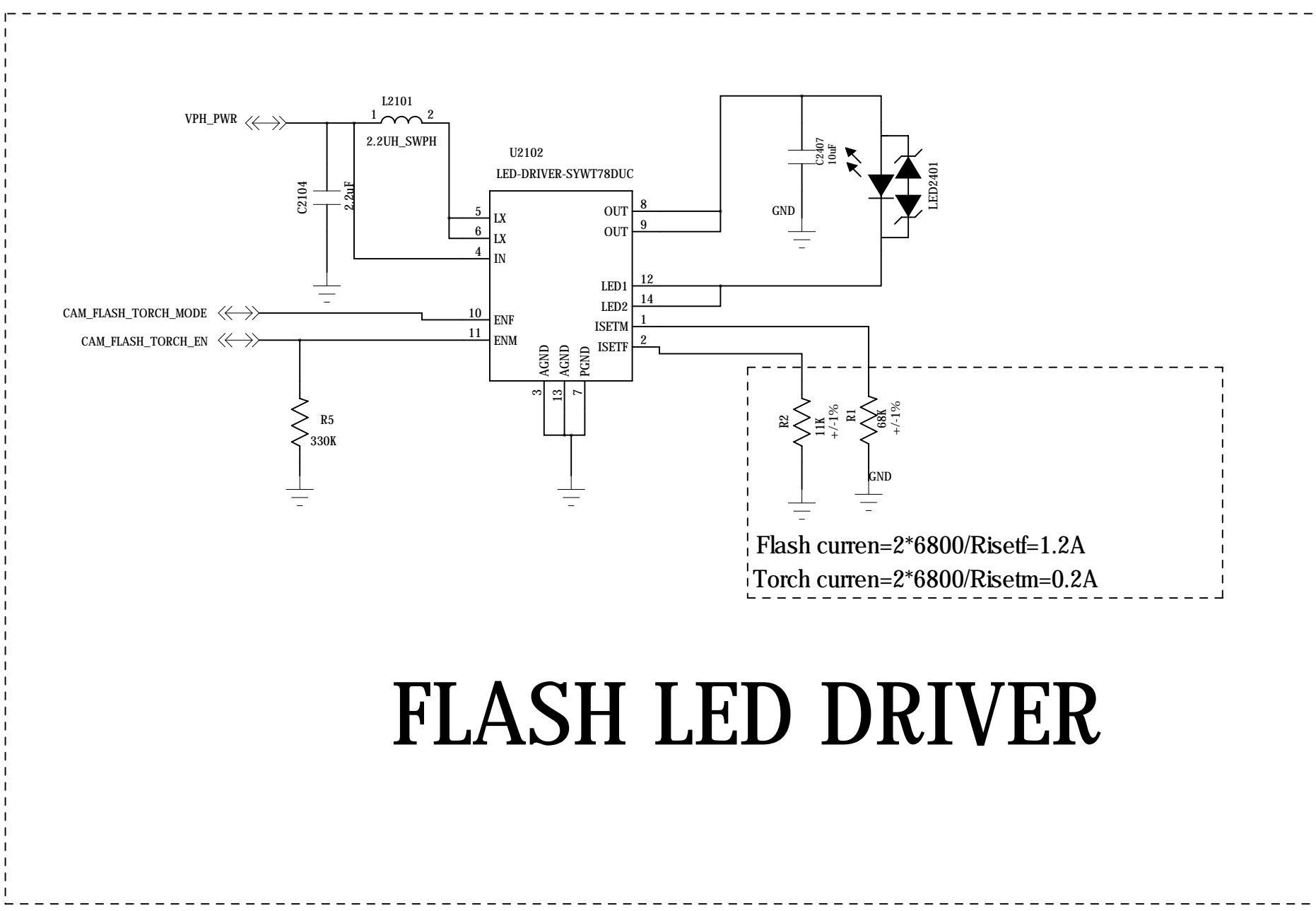
1	DGND
2	MCN
3	MCP
4	DGND
5	MDNO
6	MDPO
7	DGND
8	MDN1
9	MDP1
10	DGND
11	AVDD 2.8V
12	DGND
13	DGND
14	DGND
15	DVDD 1.2V
16	DGND
17	DOVDD 1.8V
18	DGND
19	SDA
20	SCL
21	RESET
22	DGND
23	MCLK
24	DGND

FRONT_camera

0511 update conector



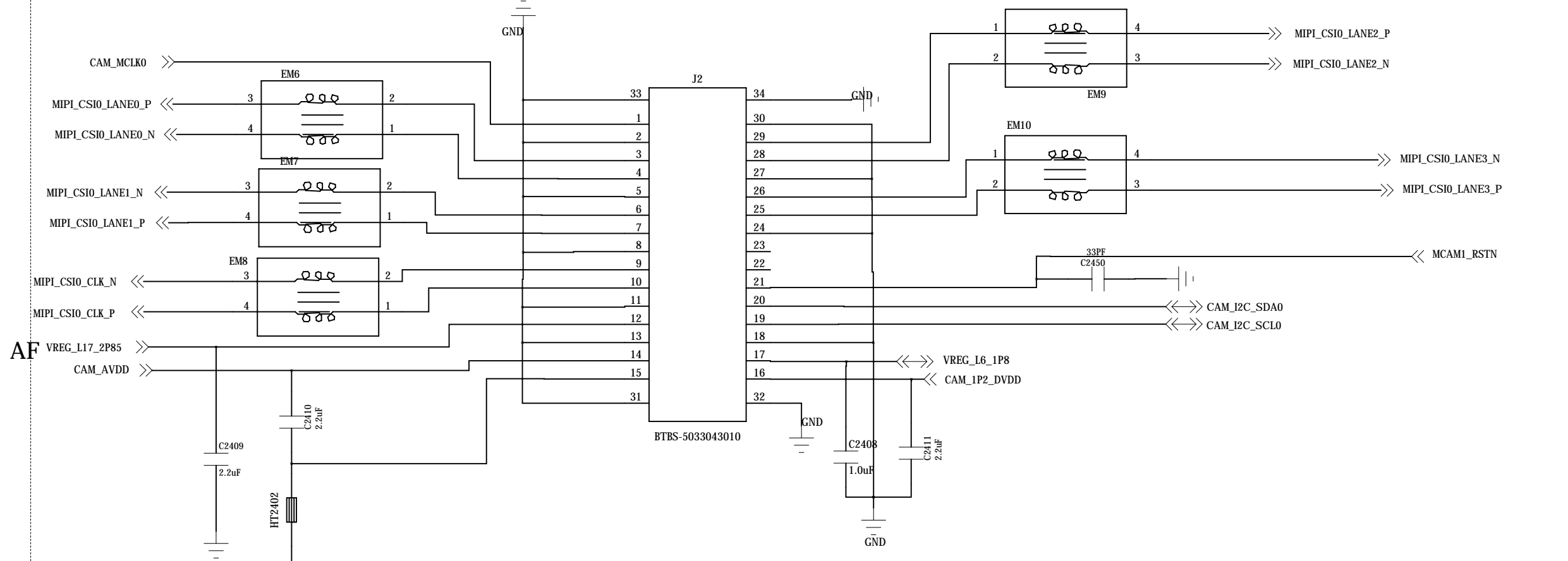
Main Camera / Sub Camera share power domain design
should double check the voltage level is compatible



FLASH LED DRIVER

PIN	
1	MCLK
2	DGND
3	MDPO
4	MDNO
5	DGND
6	MDN1
7	MDP1
8	DGND
9	MCN
10	MCP
11	DGND
12	AF_Power 2.8V
13	AF_GND
14	AVDD 2.8V
15	AGND
16	DVDD 1.2V
17	DOVDD 1.8V
18	DGND
19	SIO_C
20	SIO_D
21	RESET
22	VPP NC
23	AF_EN NC
24	DGND
25	MDP3
26	MDN3
27	DGND
28	MDN2
29	MDP2
30	DGND

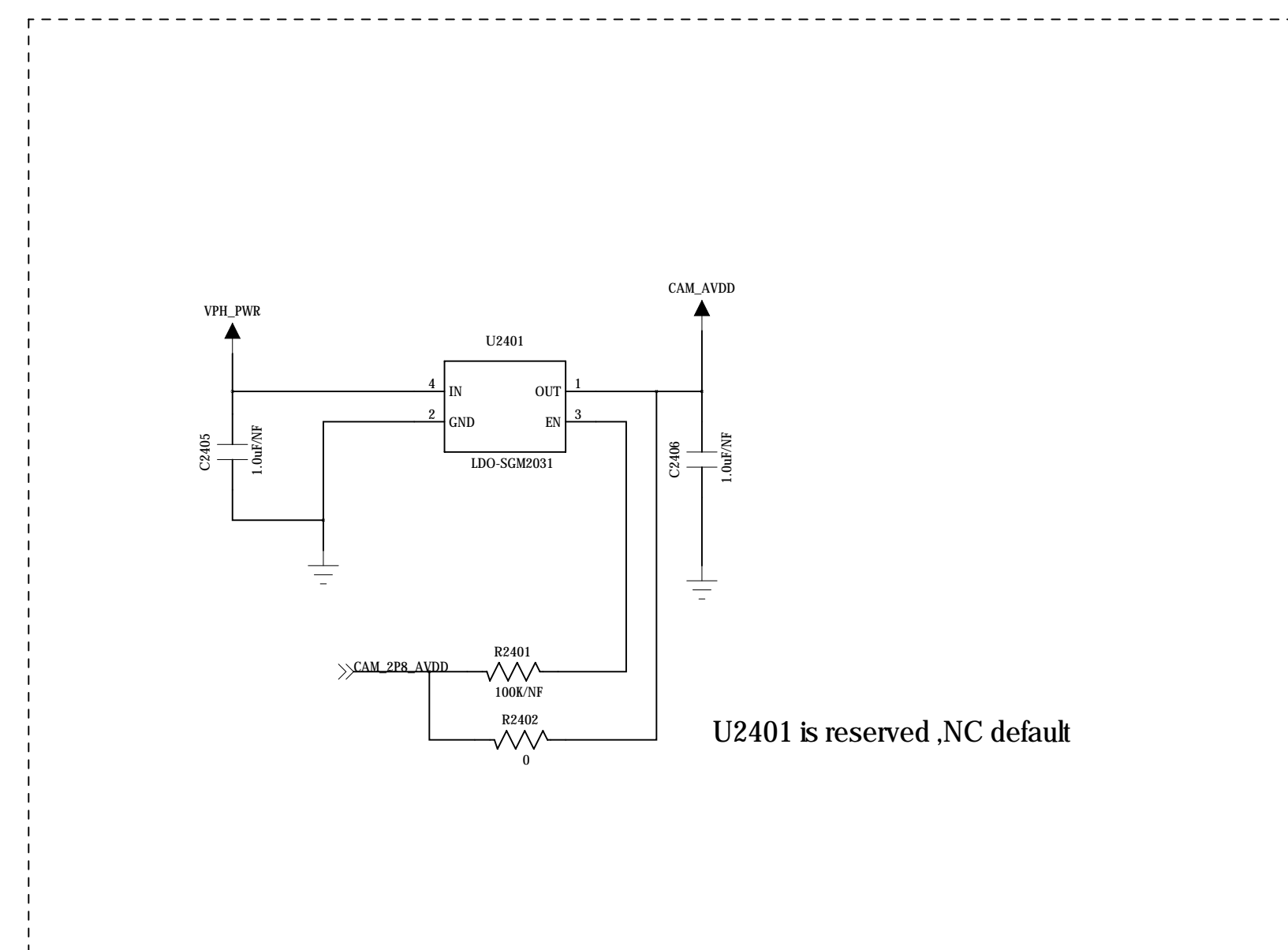
0711 update conector



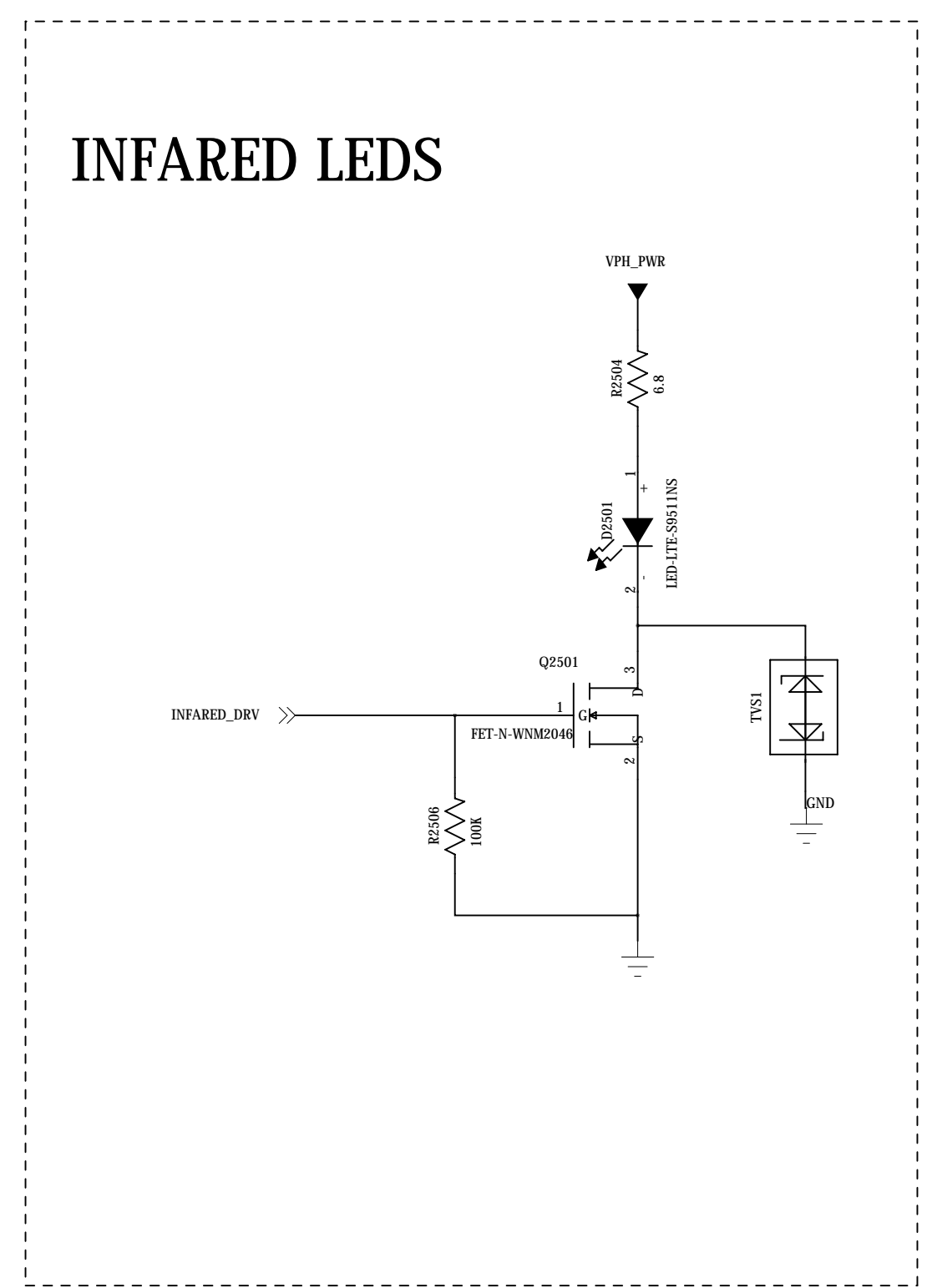
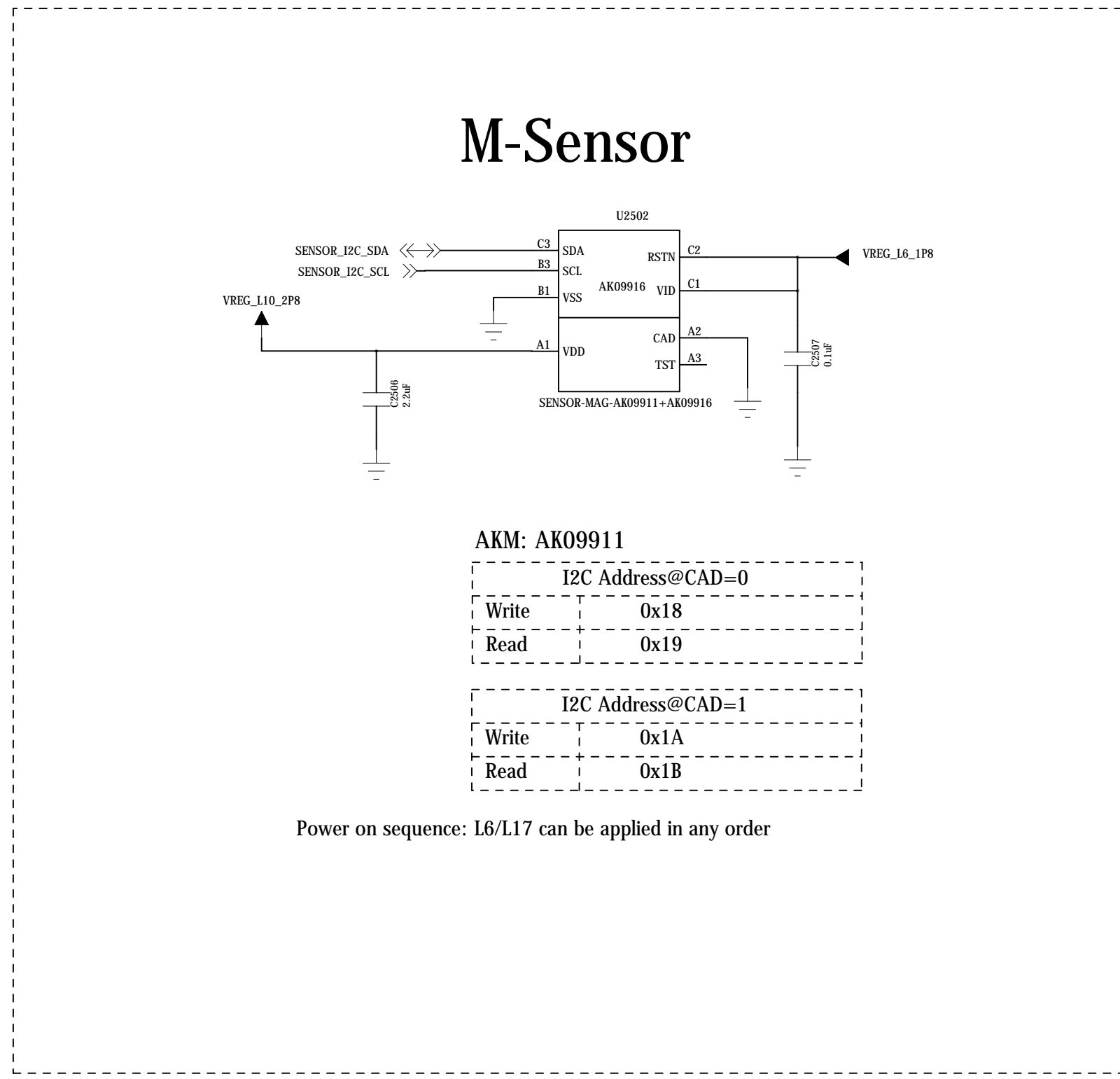
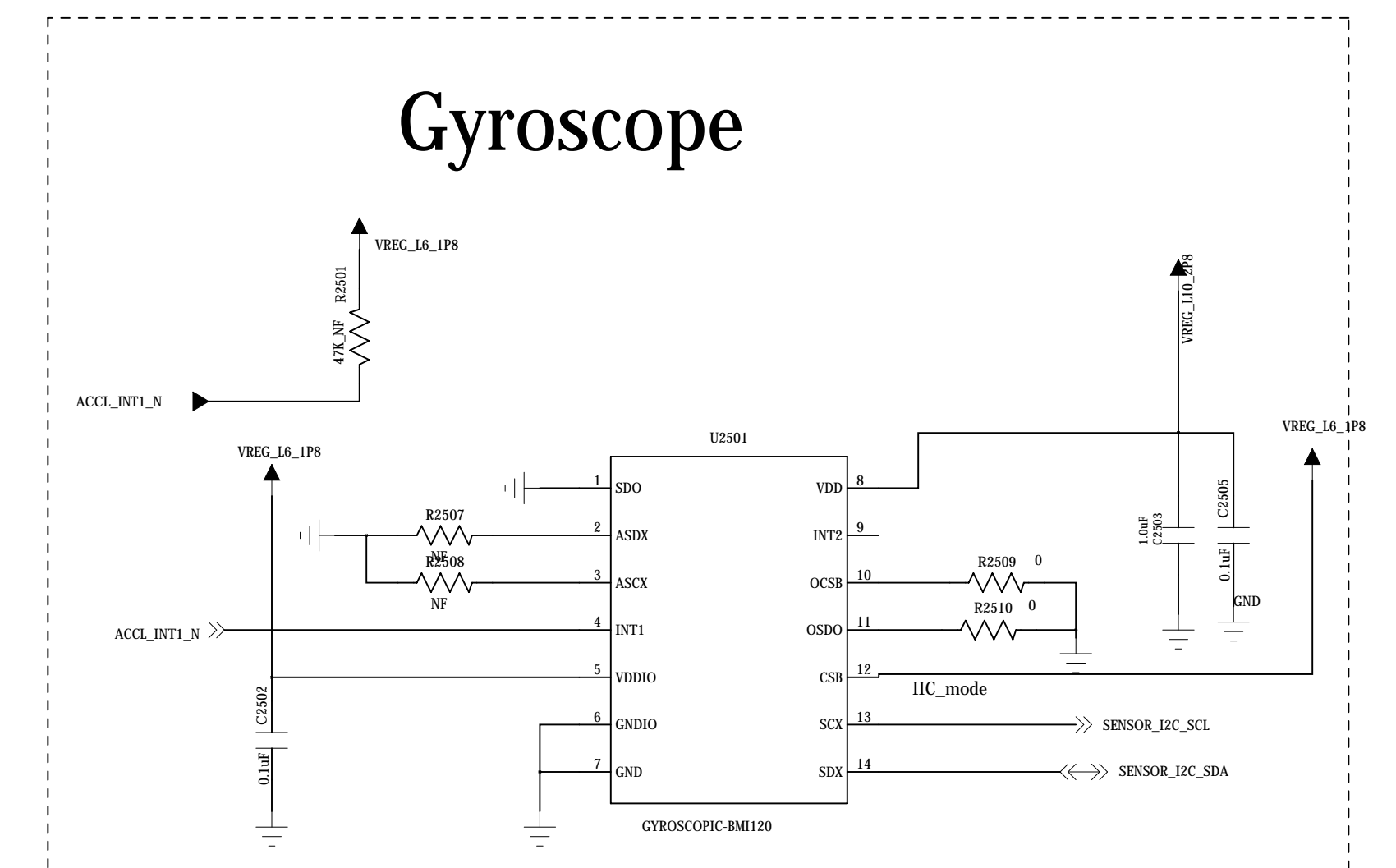
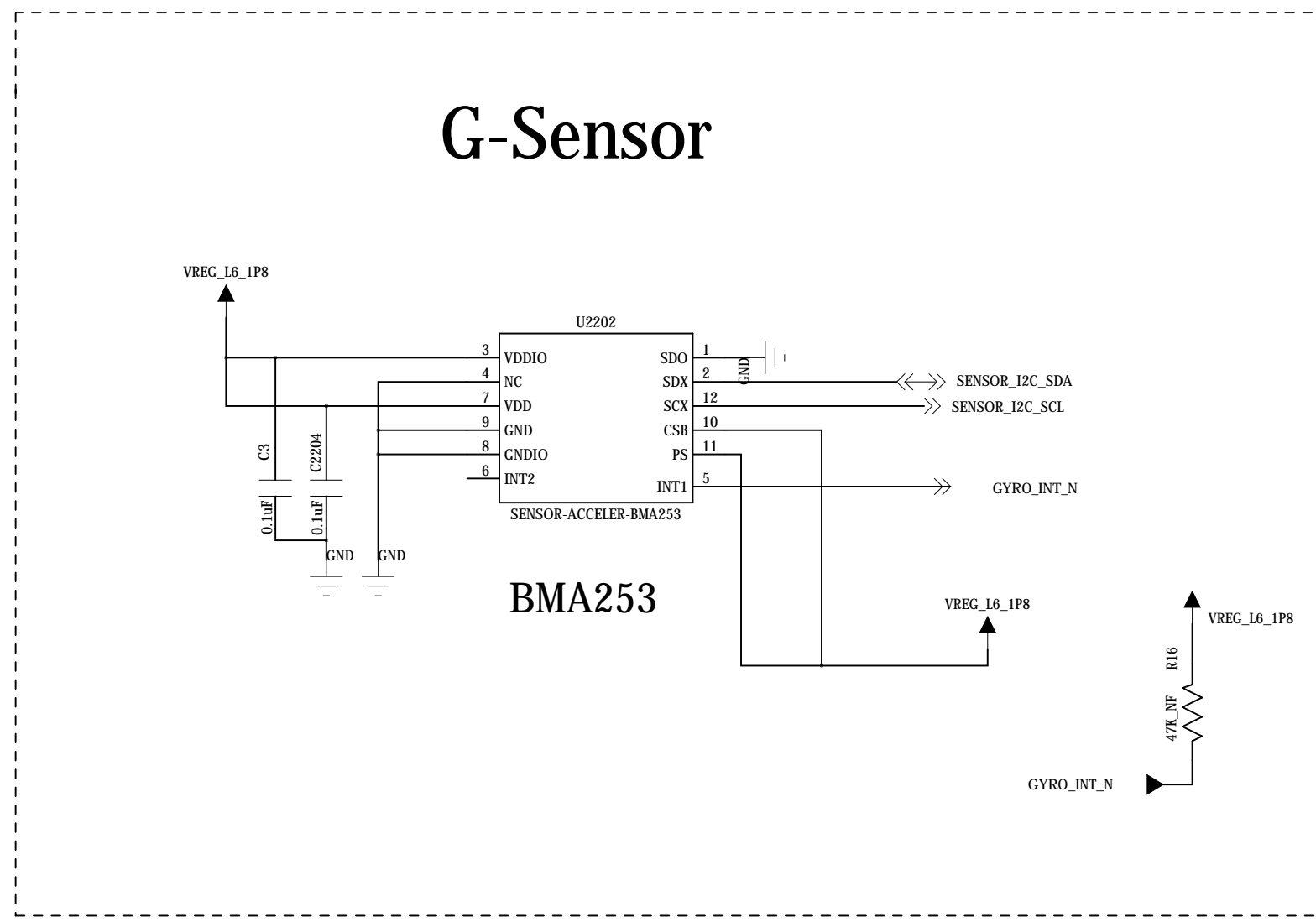
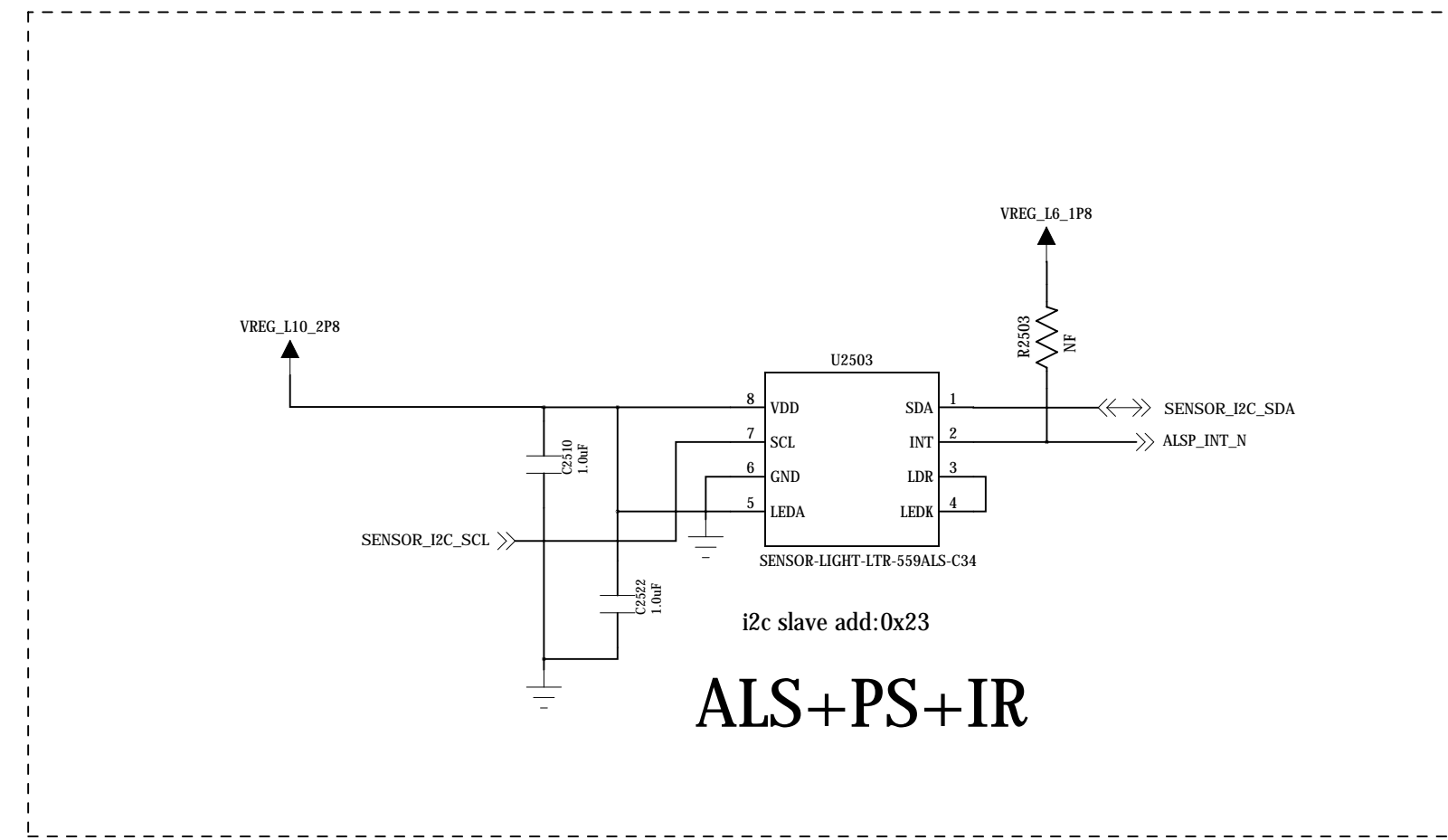
Main Camera

Rear Camera: 8Mp
Module: OV8865
Sensor: OV8865
Power on sequence: L6(DOVDD) must before L17(AVDD)

I2C Address	
Write	0x6C
Read	0x6D



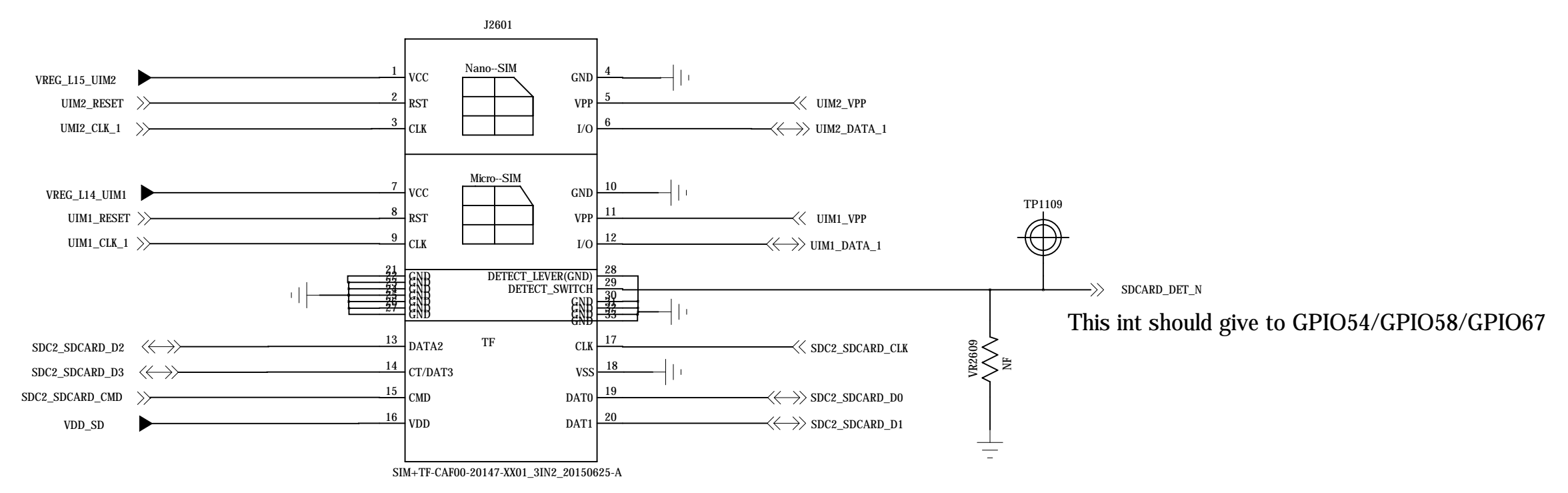
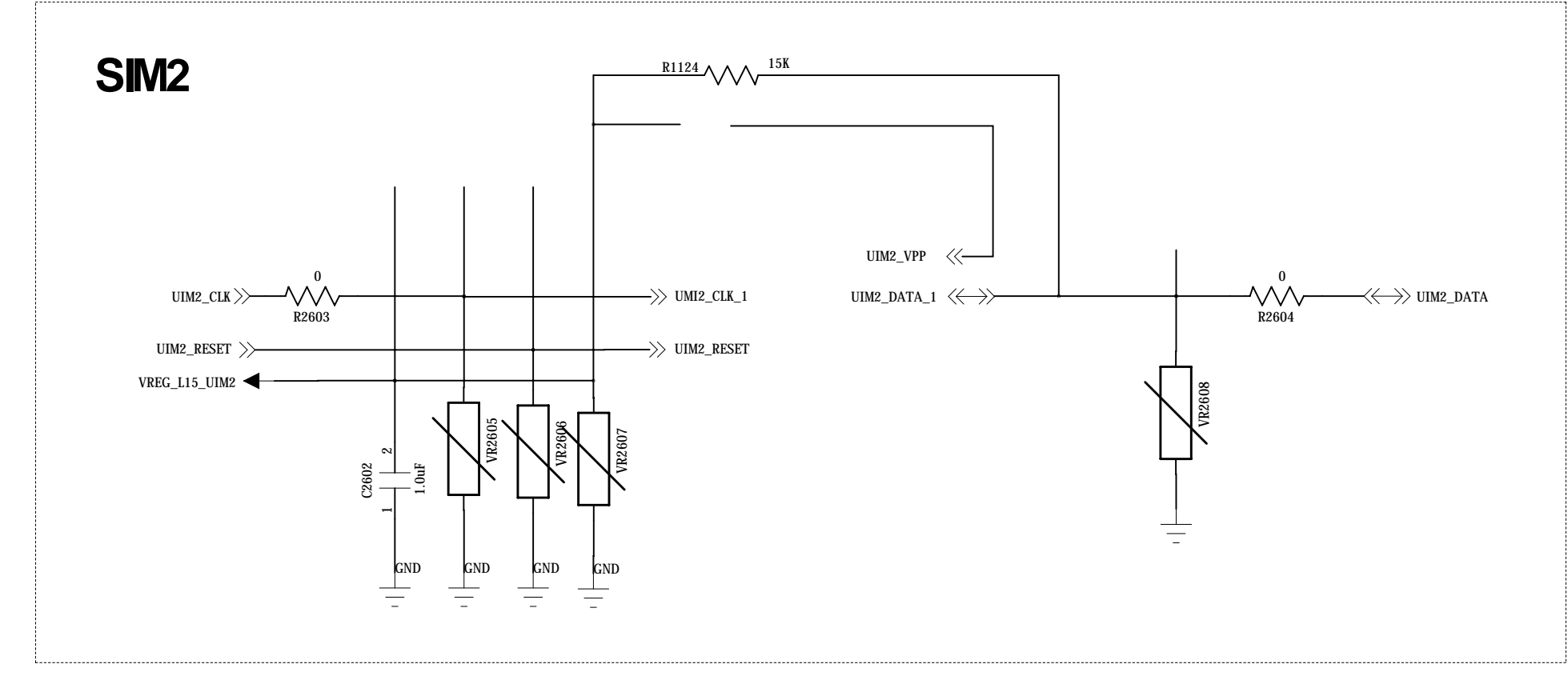
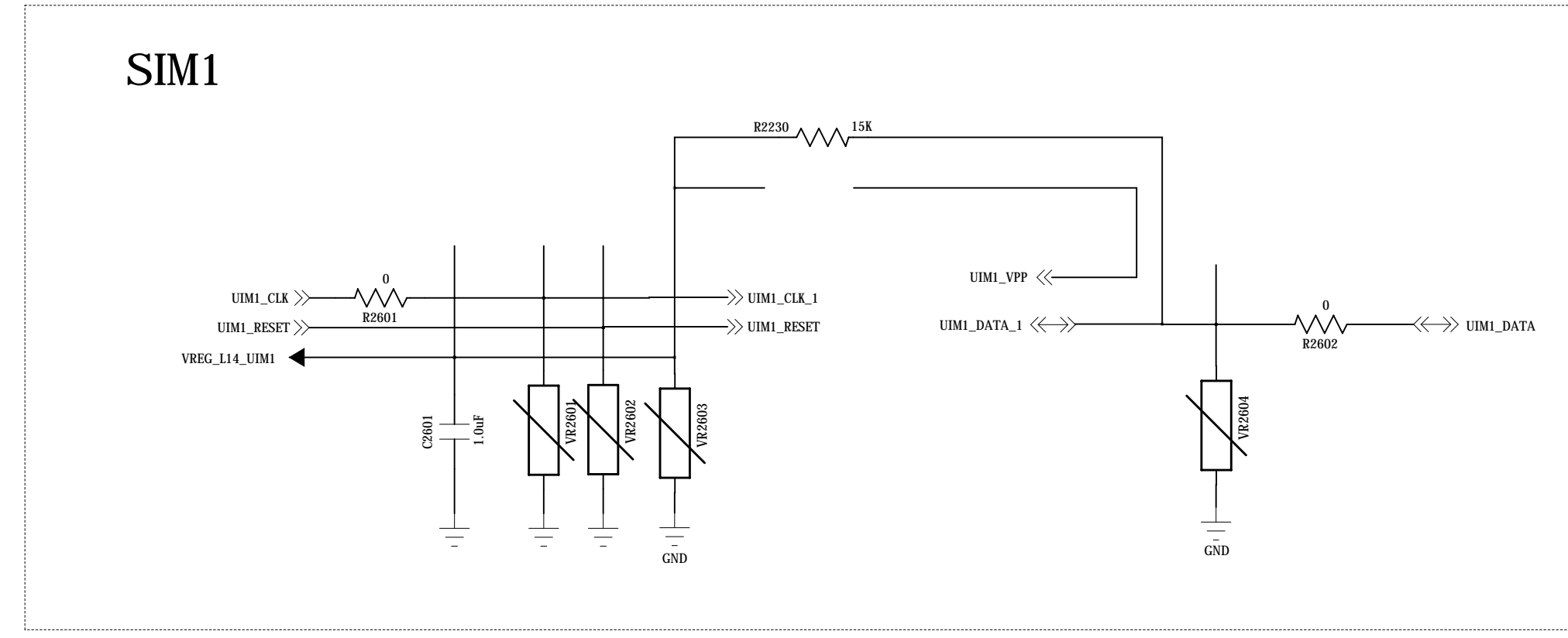
Main/Slave Camera and Flash



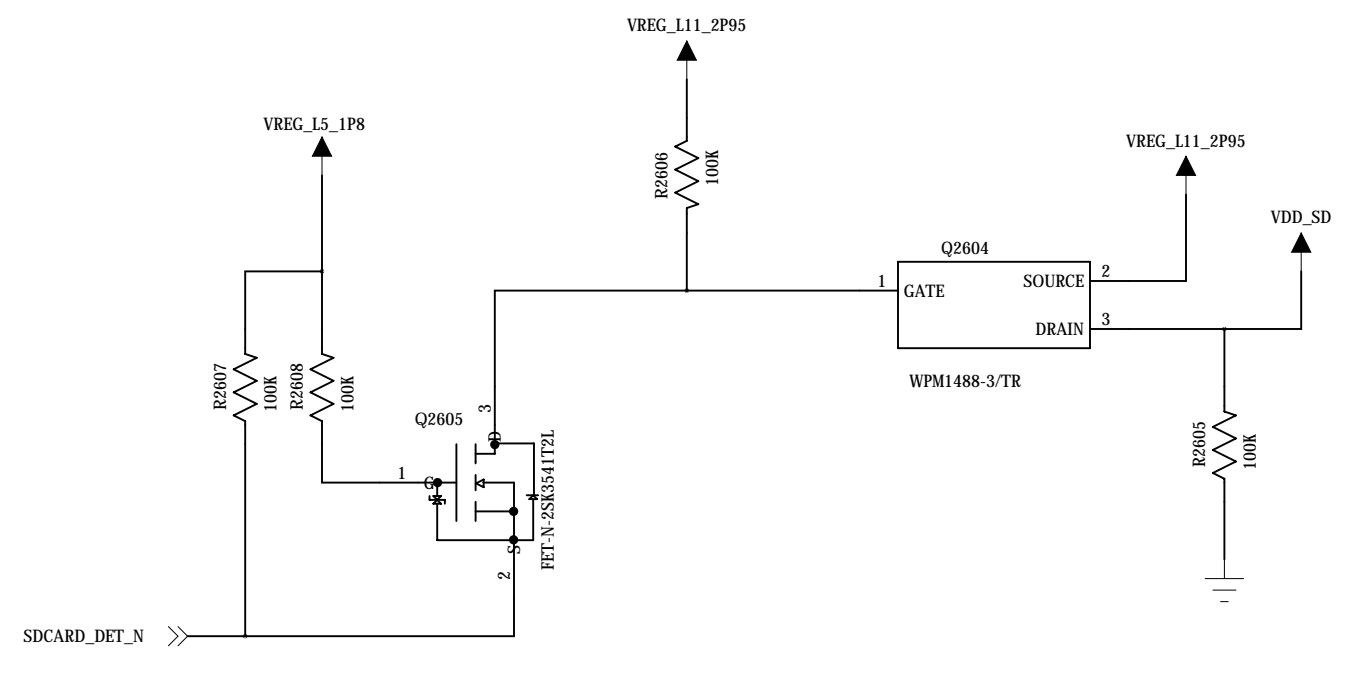
- BMI160**
SD0=0 7b1101000 0x68
SD0=1 7b1101001 0x69
- LSM6DS3**
SD0=0 7b1101010 0x6A
SD0=1 7b1101011 0x6B

Power on sequence: L6/L17 can be applied in any order

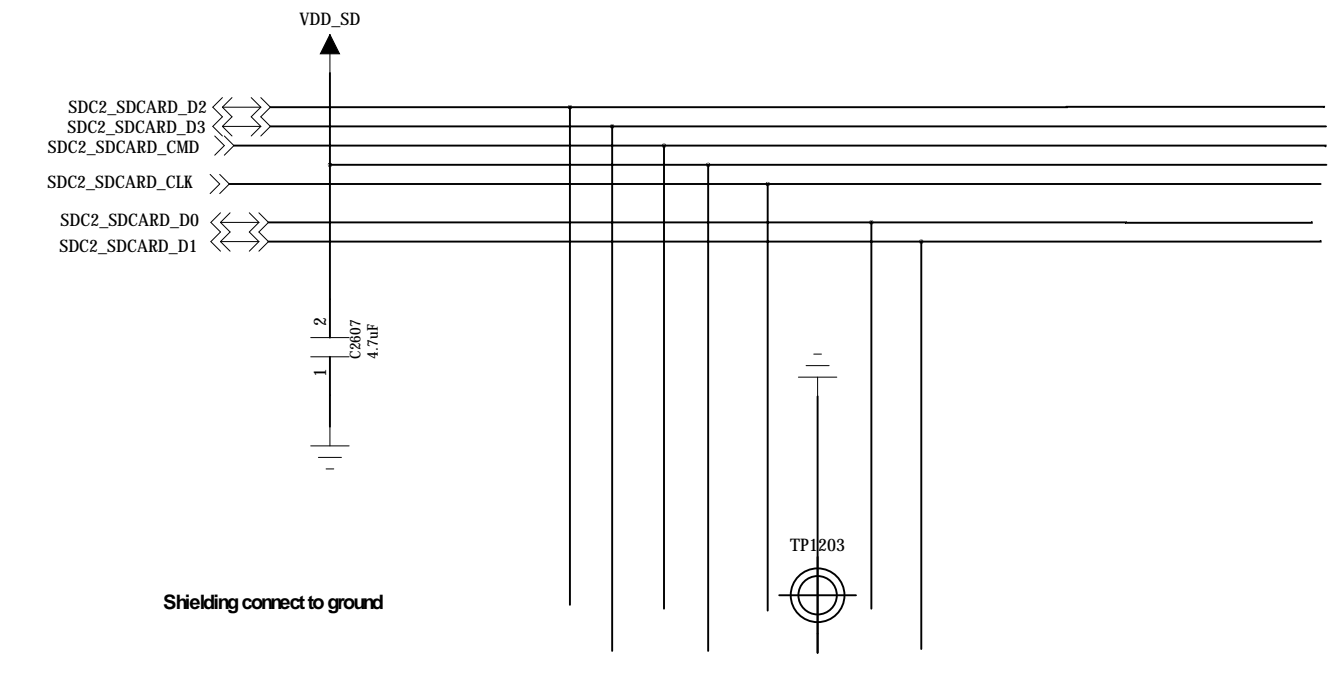
SENSORS



Vout=3.0V, I-lim=1A

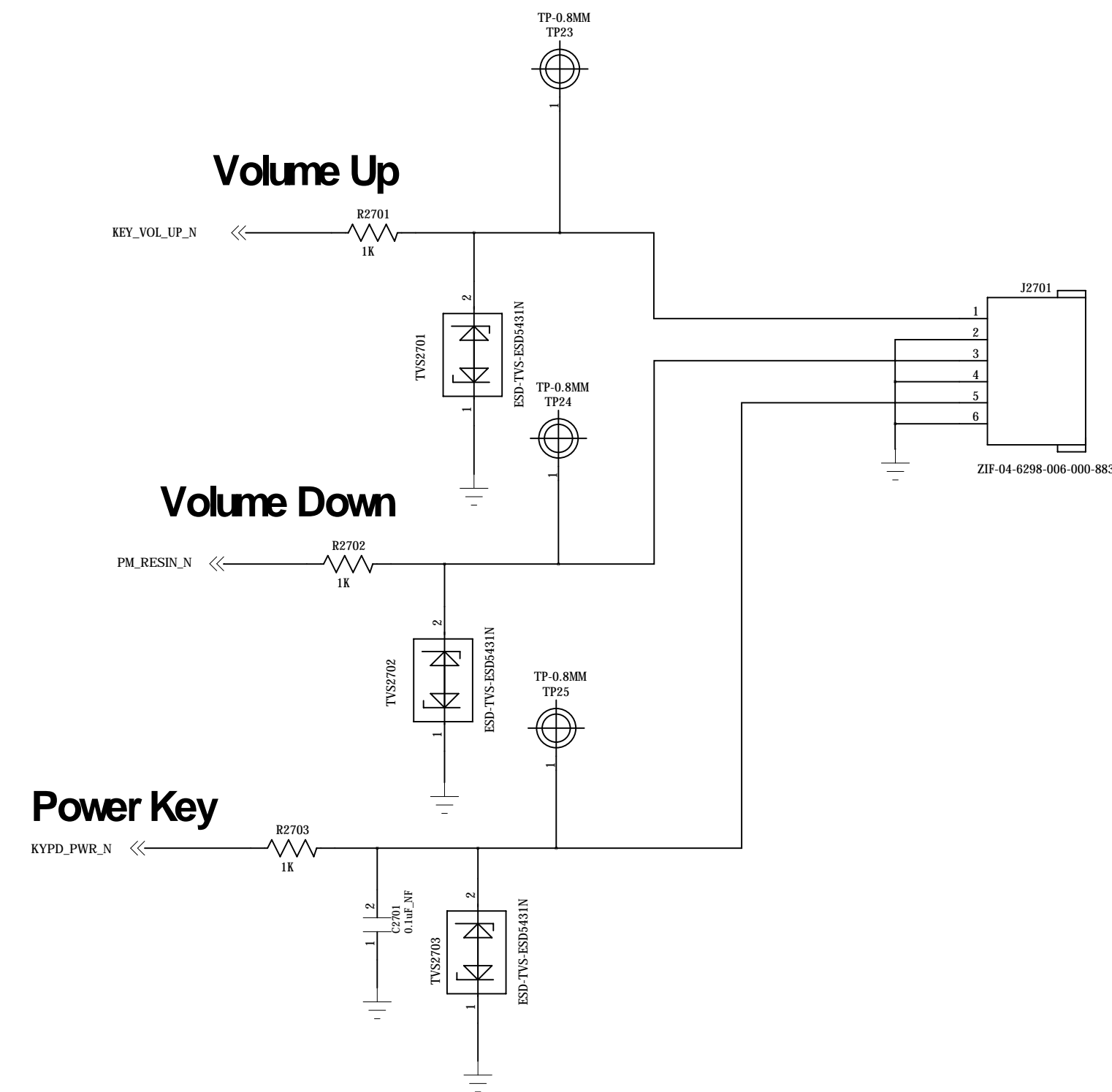


SD CARD



SIM/TF card

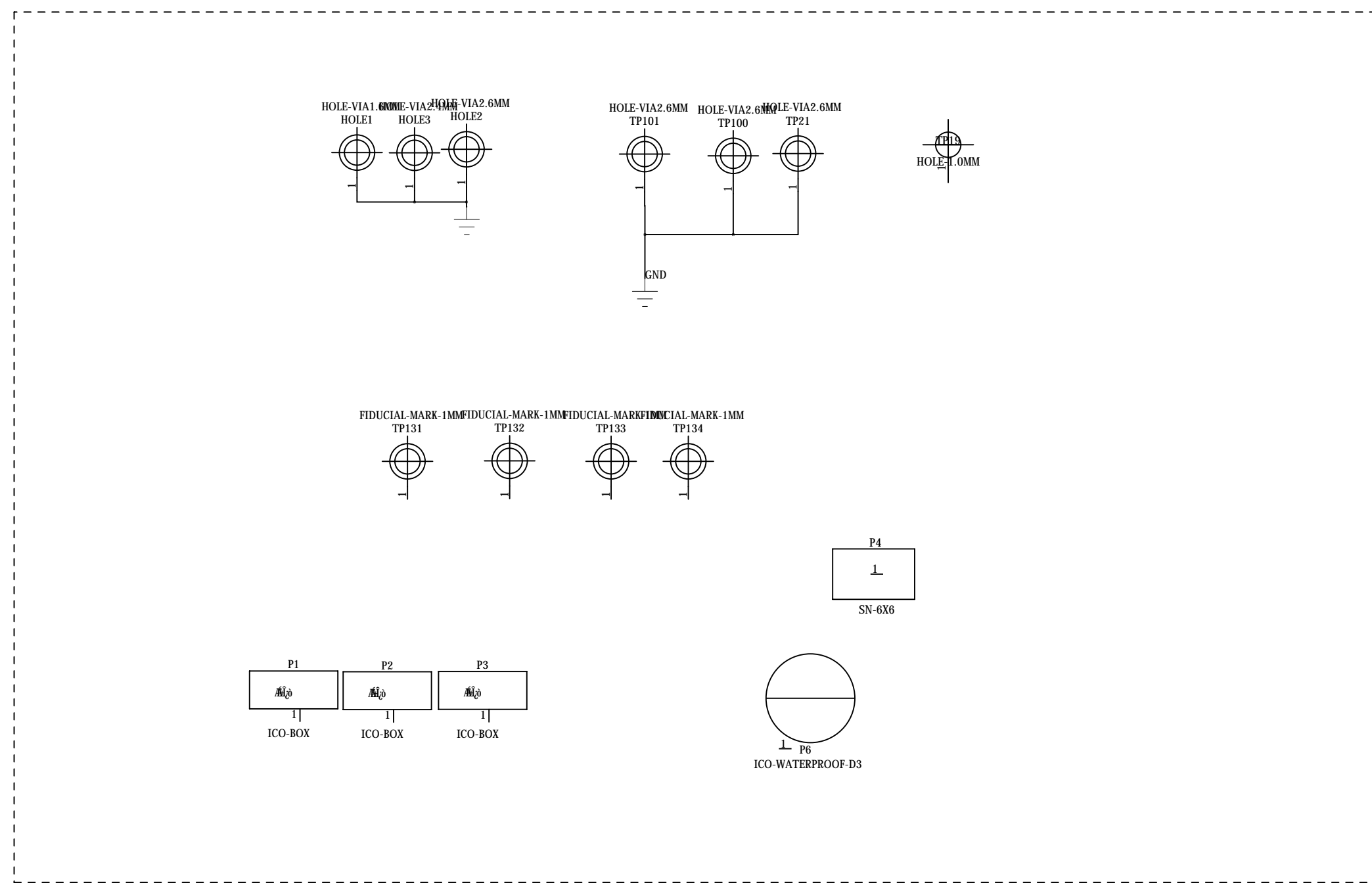
Signal	Description
KEY_VOL_UP_N	Volume Up
PM_RESIN_N1	Volume Down
KYPD_PWR_N1	POWER_ON
PM_RESIN_N1 + KYPD_PWR_N1	Hardware Reset



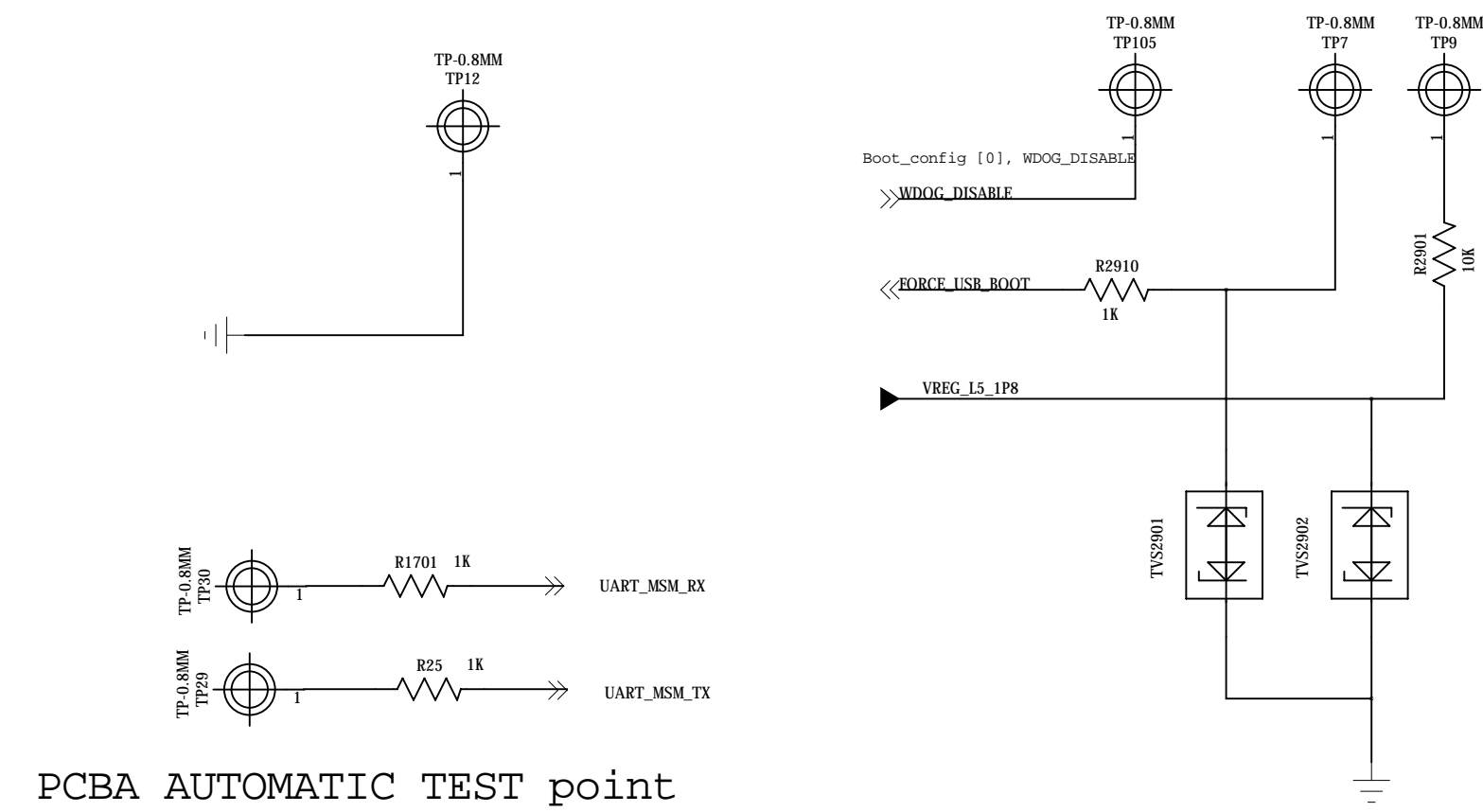
Keypad/LED/Status indicator

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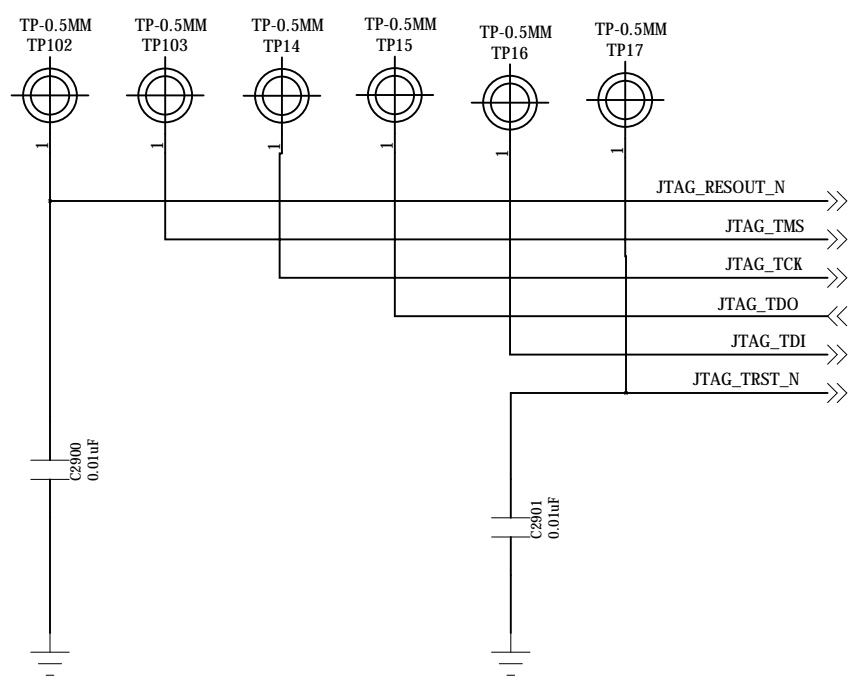
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Test Point

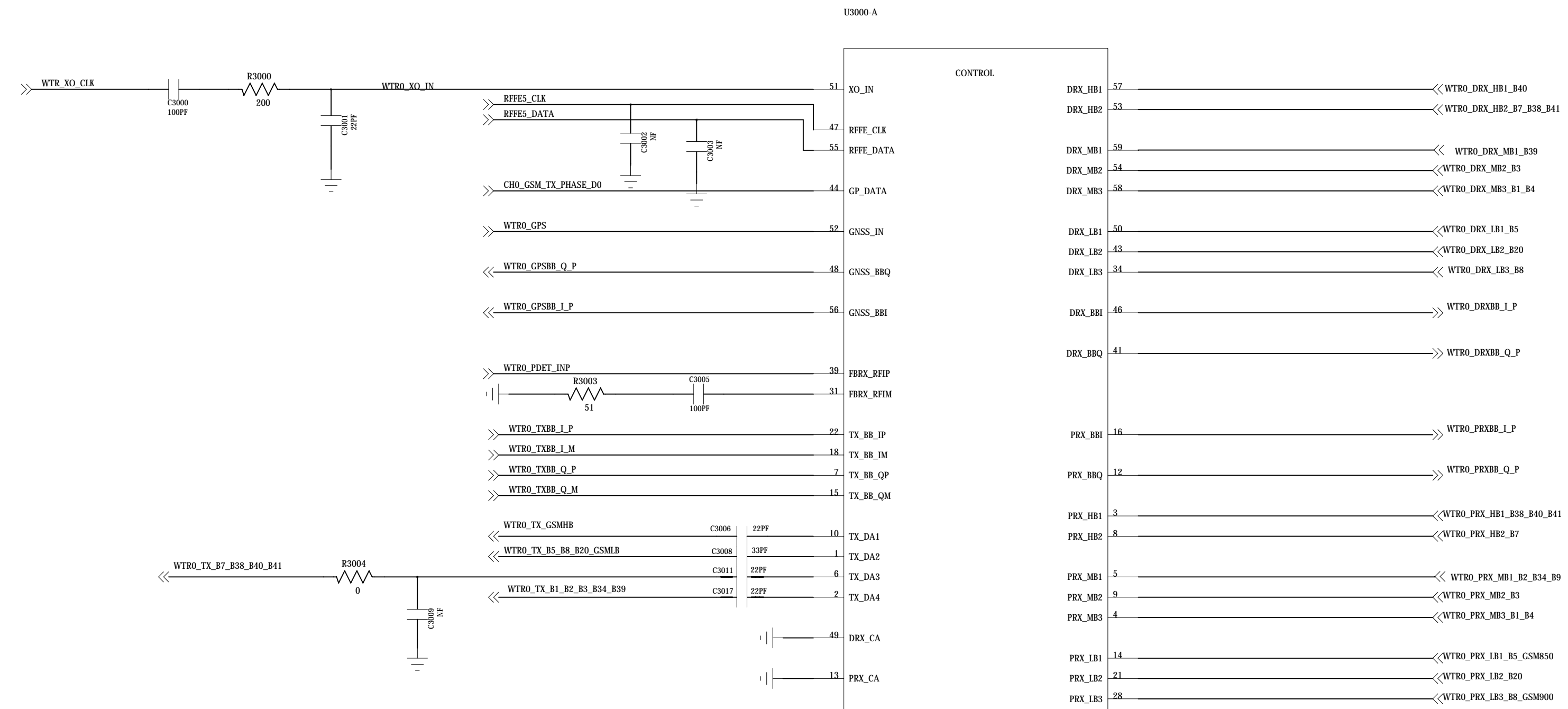


PCBA AUTOMATIC TEST point

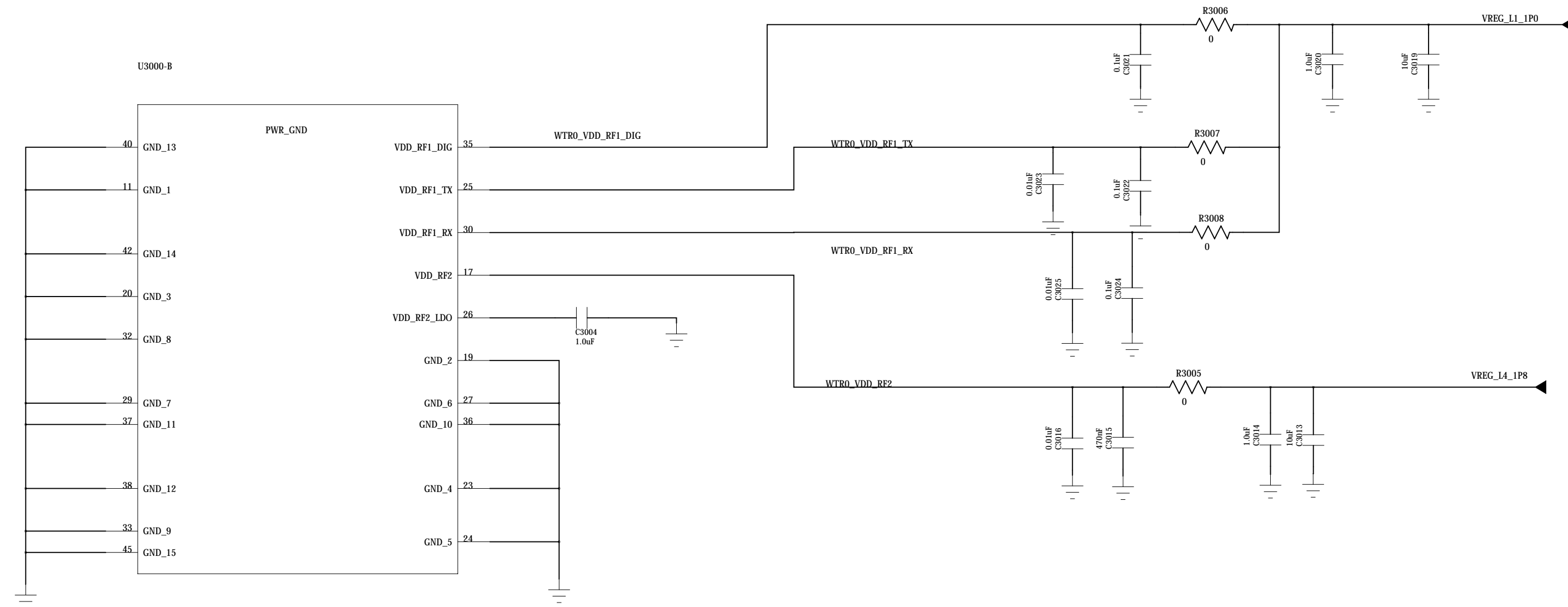


JTAG CONNECTOR

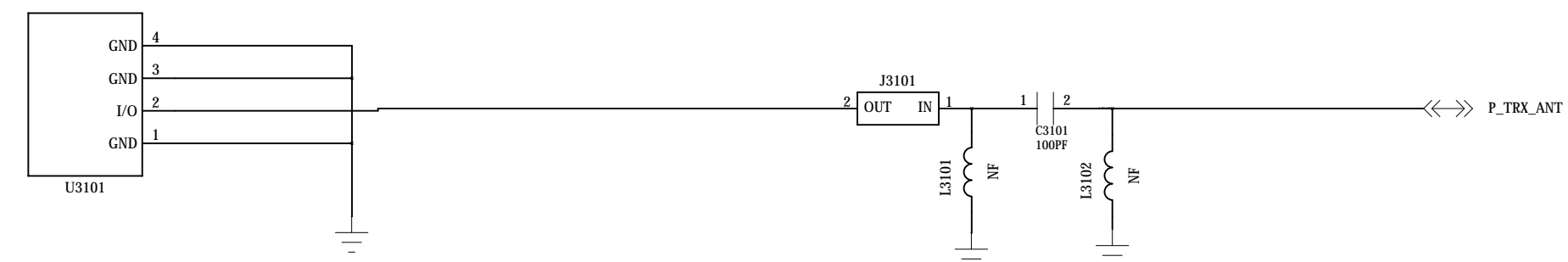
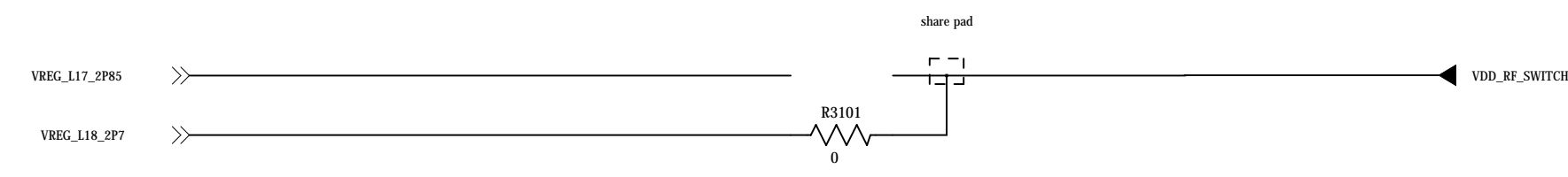
Test Point/Shields



Note:RX ports have DC at the pin,
so it need DC block, please make sure
there is no DC short to other voltages and GND



WTR 2955



Band7

Band40

Band39

Band1

Band3

Band4

Band2

Band5

Band8

Band20

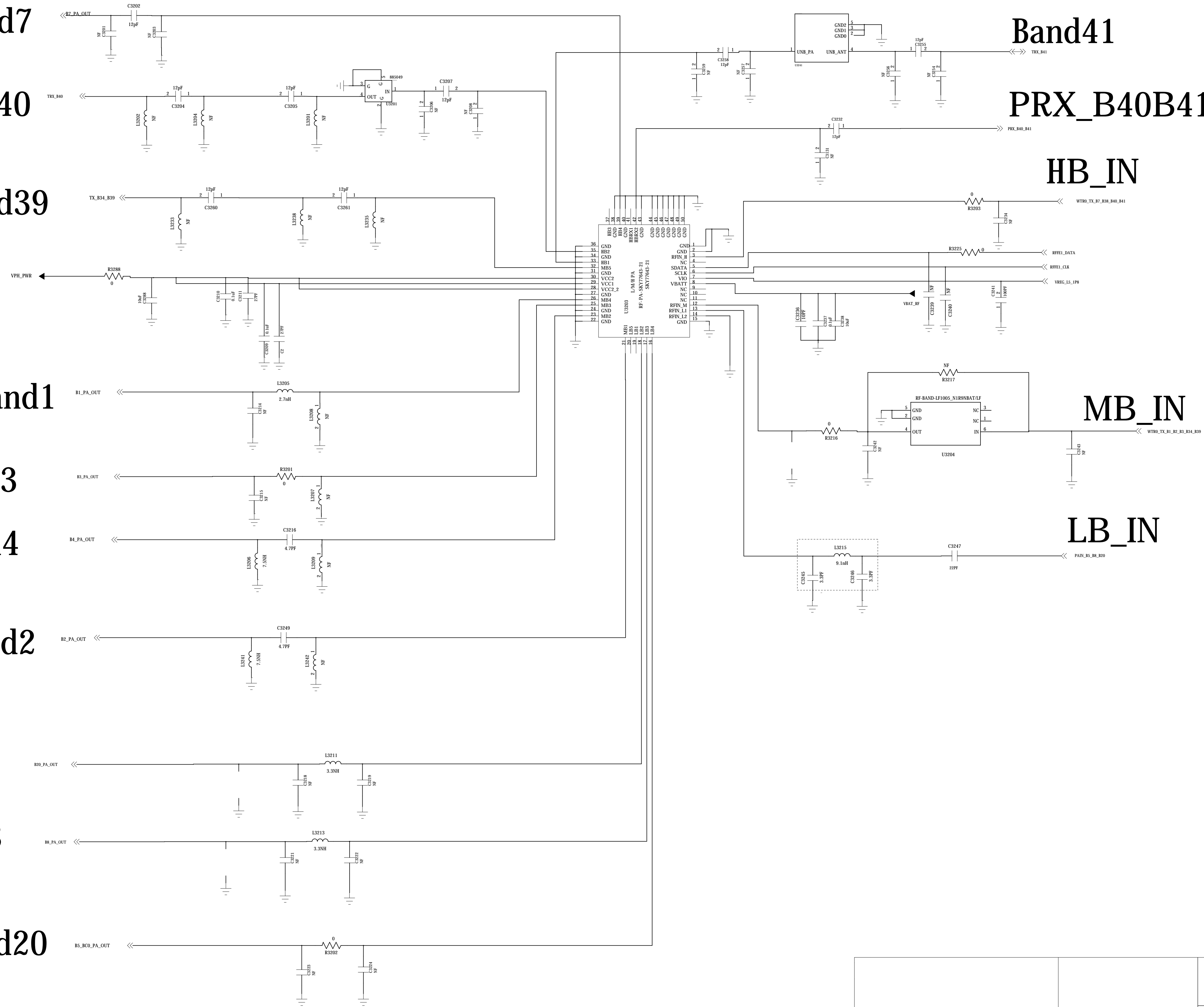
Band41

PRX_B40B41

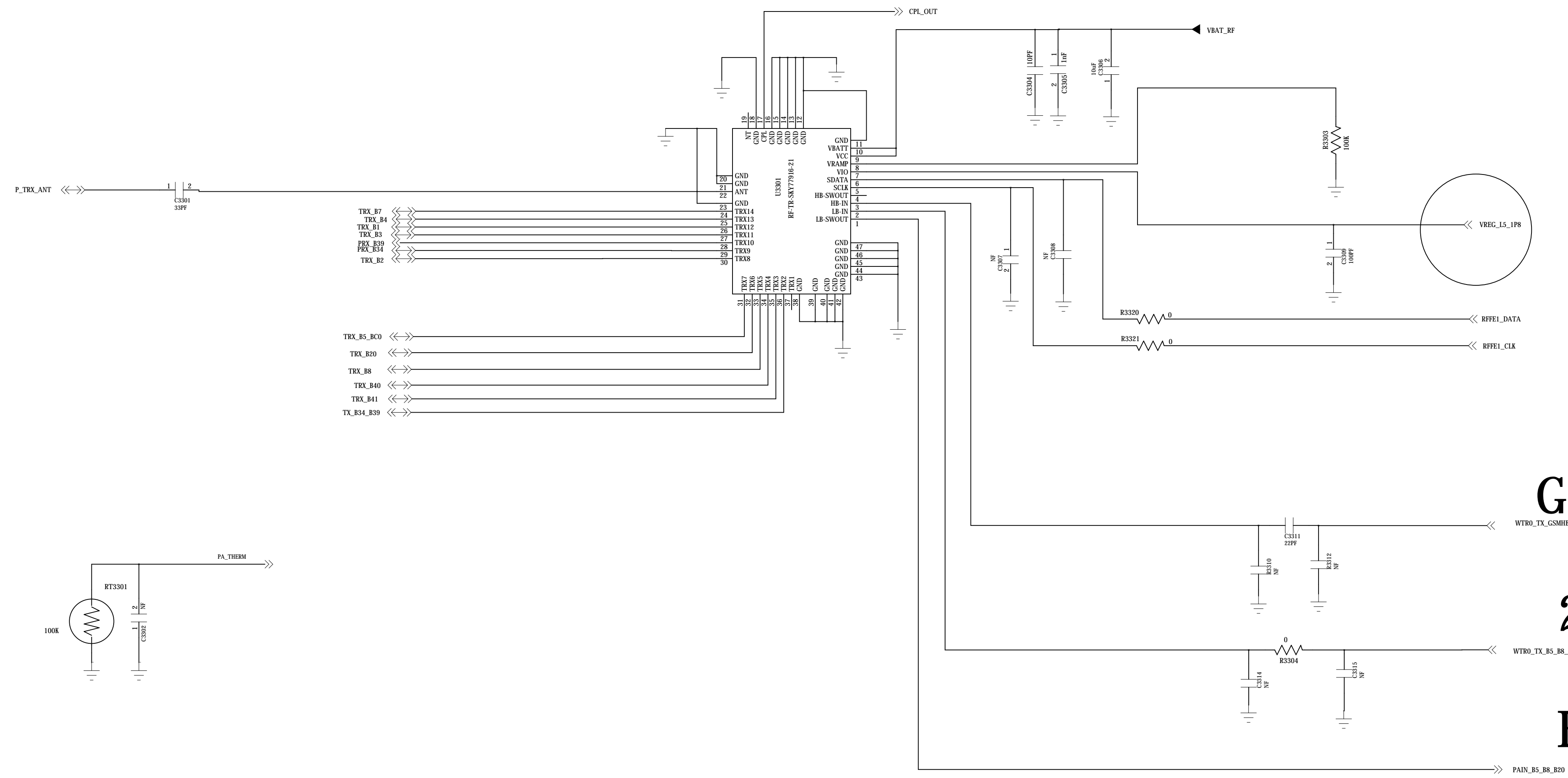
HB_IN

MB_IN

LB_IN



Title		
Sheet		
Size	Name	Rev
Date:		Sheet of

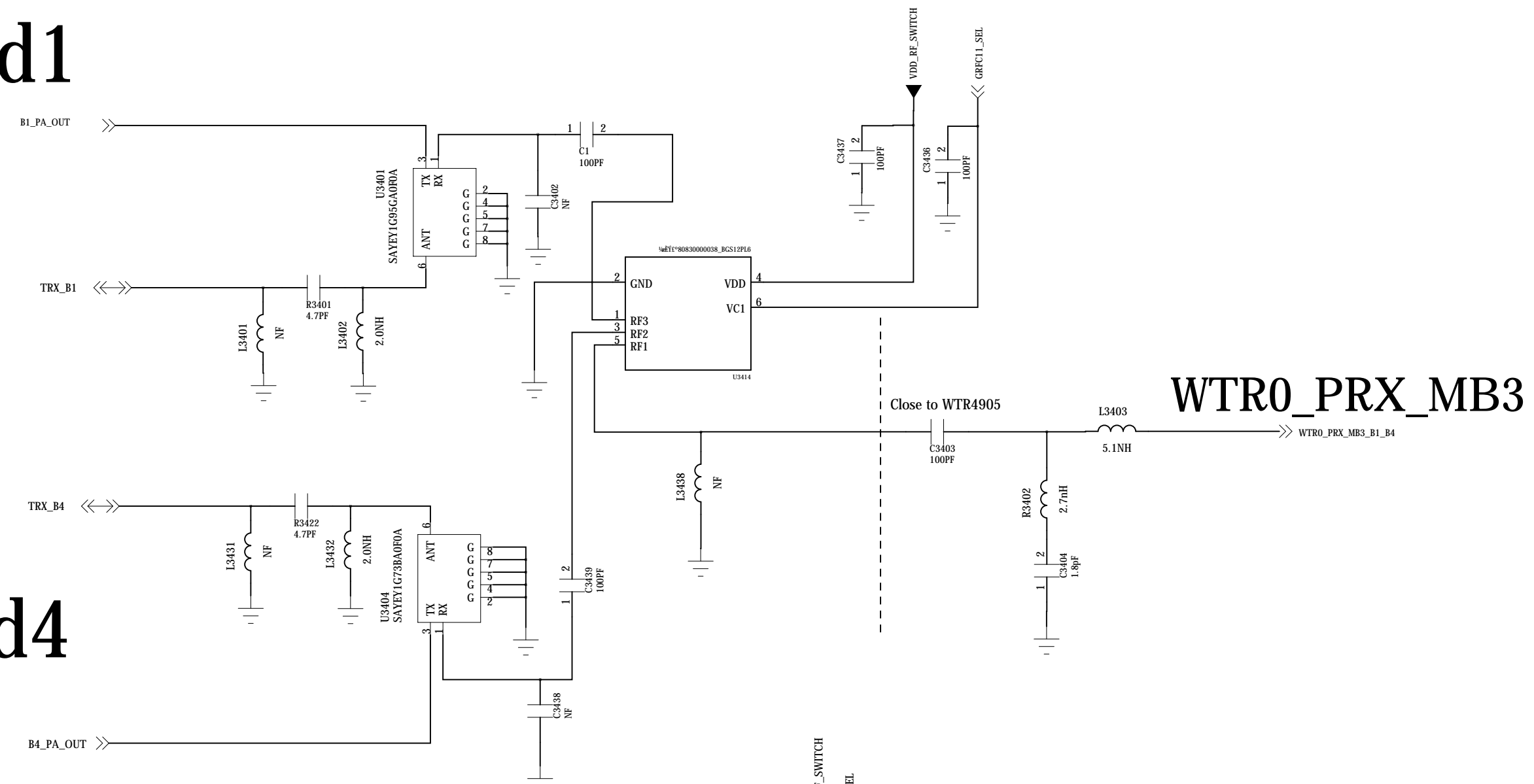


GSM_HB

2G3G4G_LB

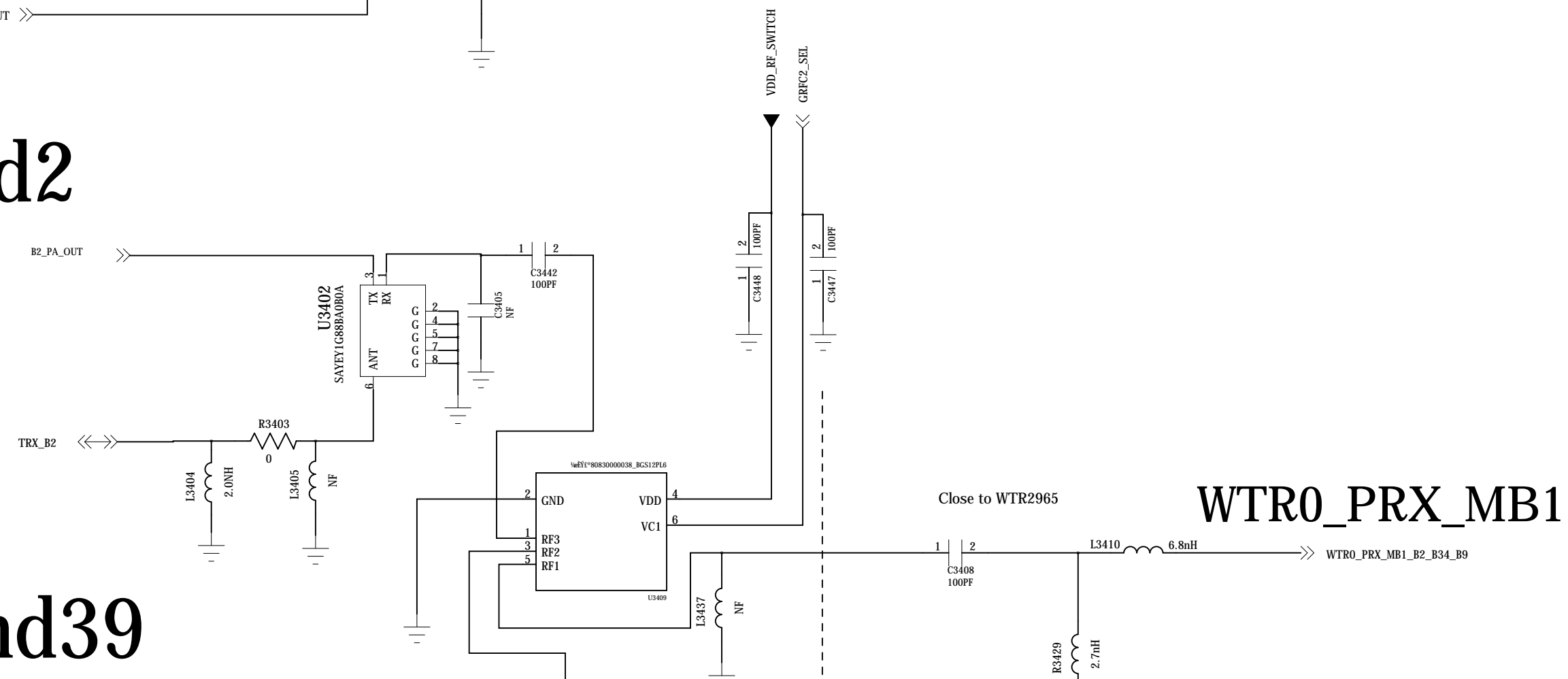
B5_B8_B20

Band1

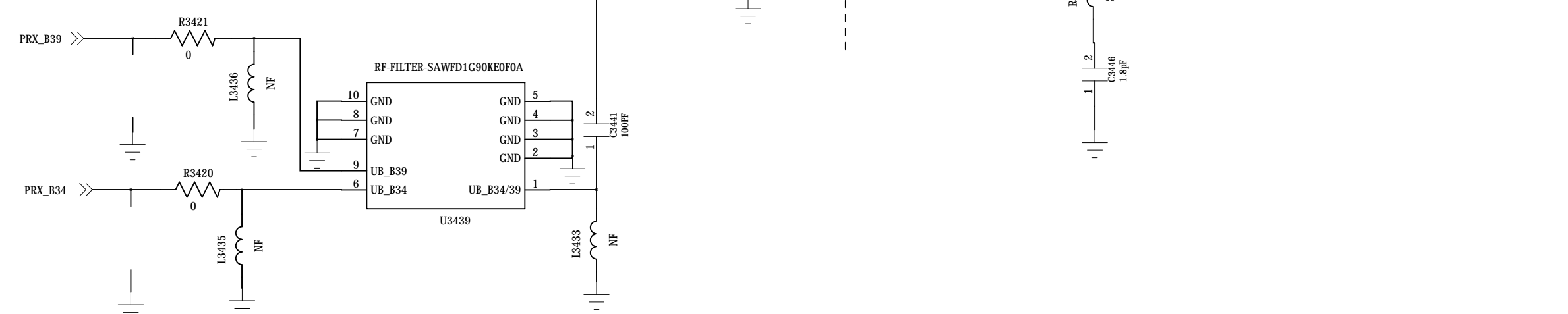


Band4

Band2

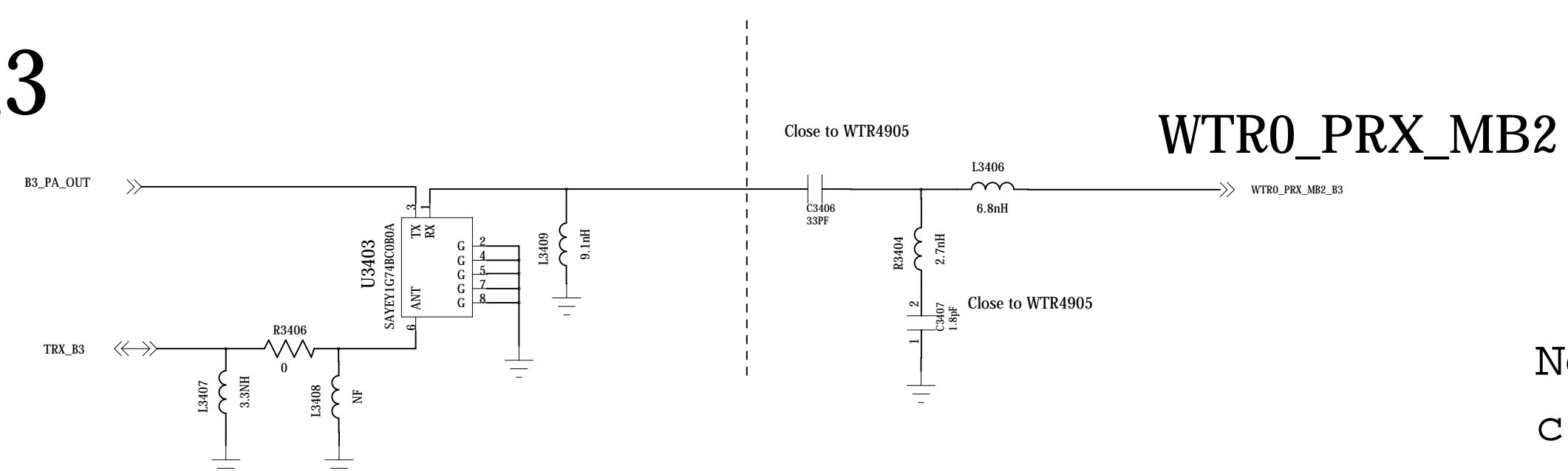


Band39

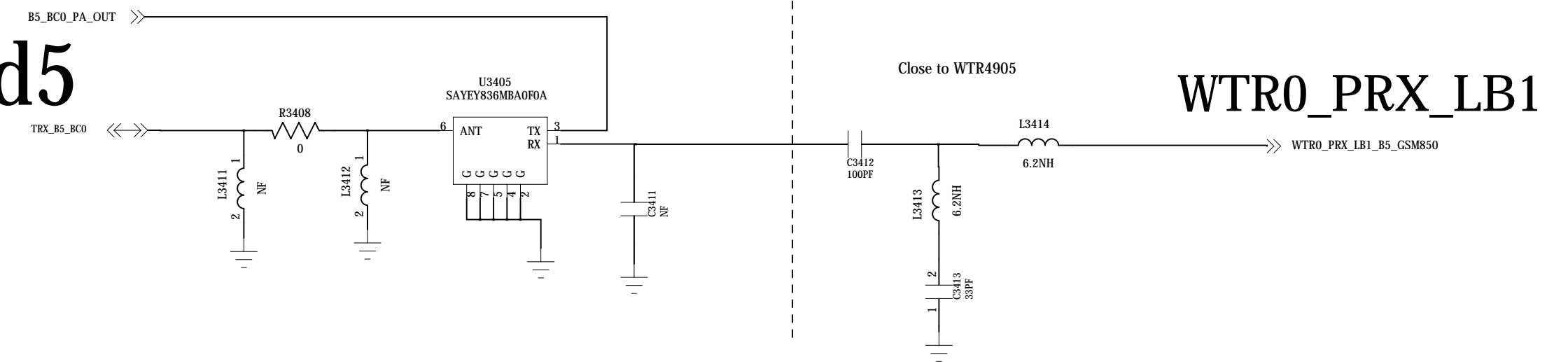


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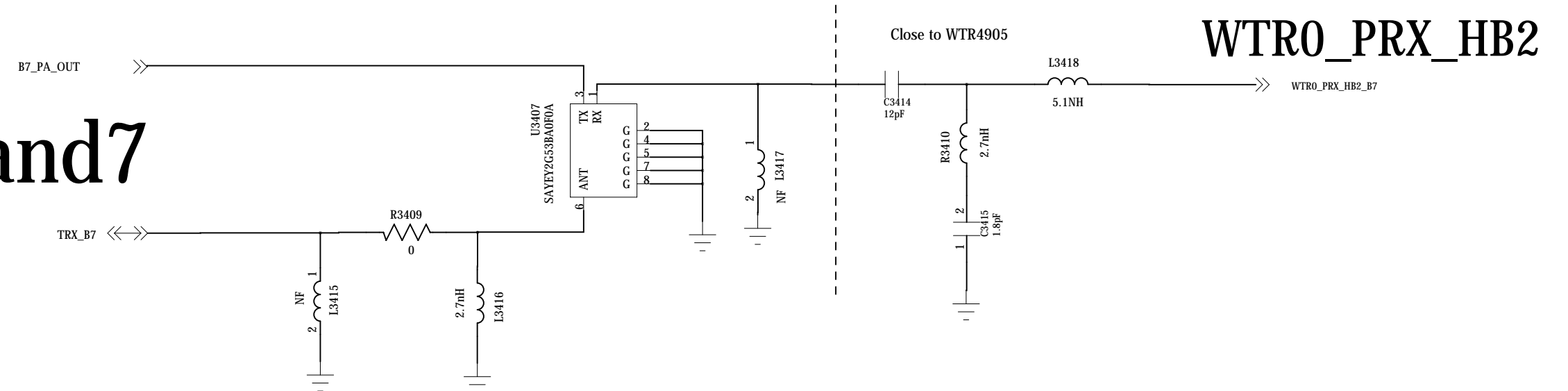
Band3



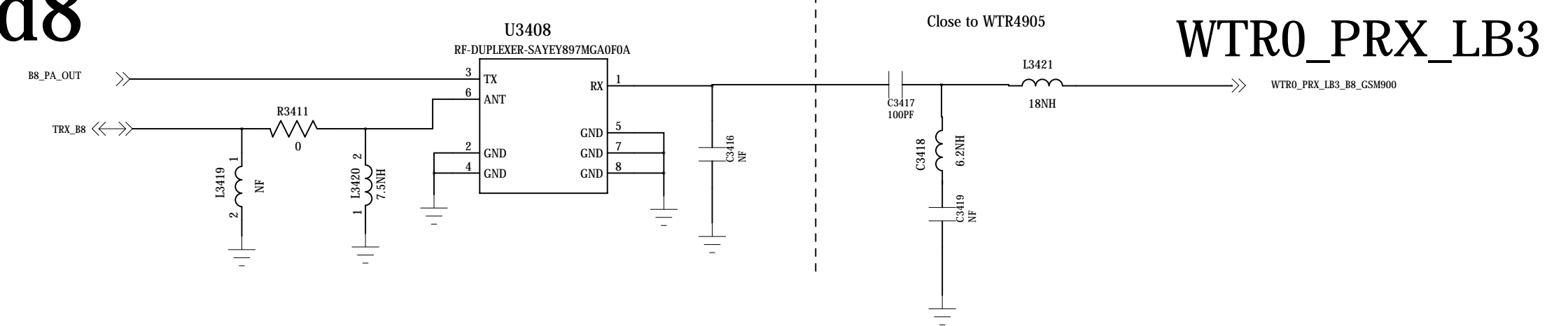
Band5



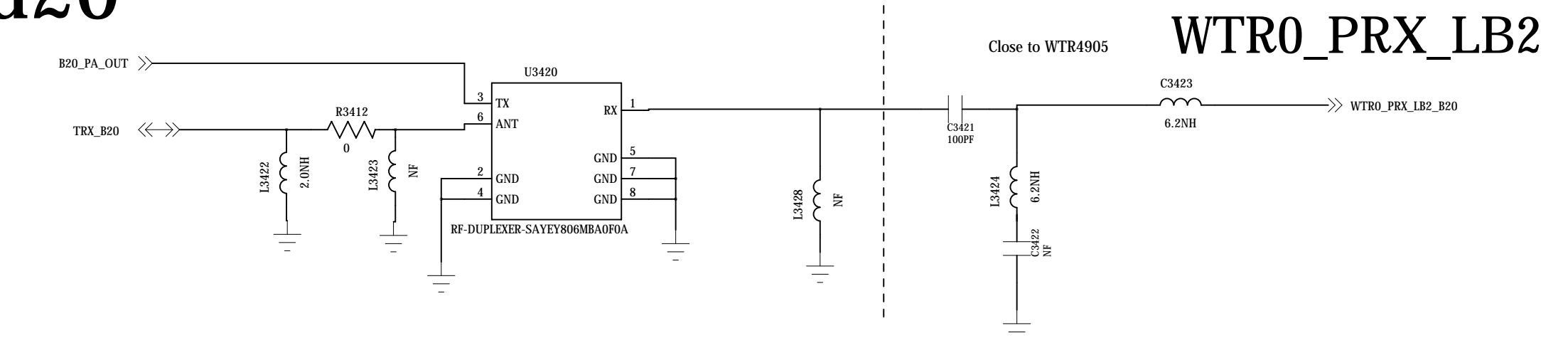
Band7



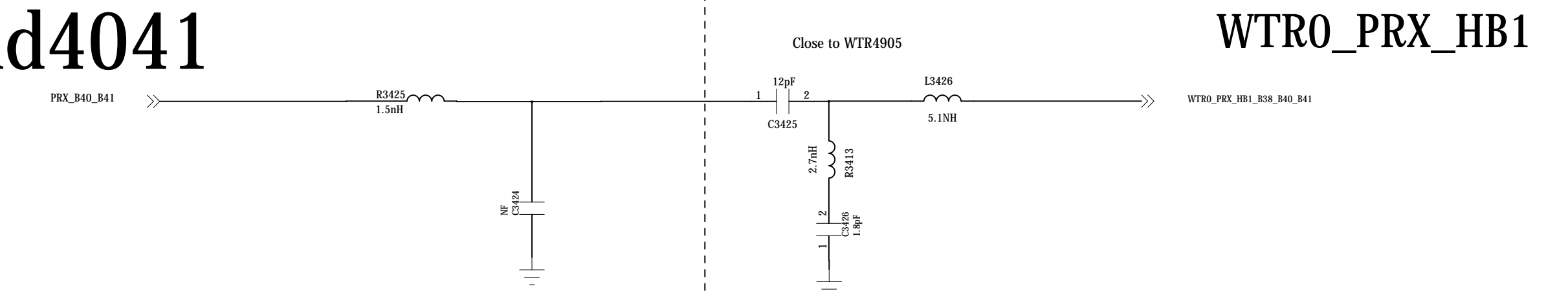
Band8



Band20

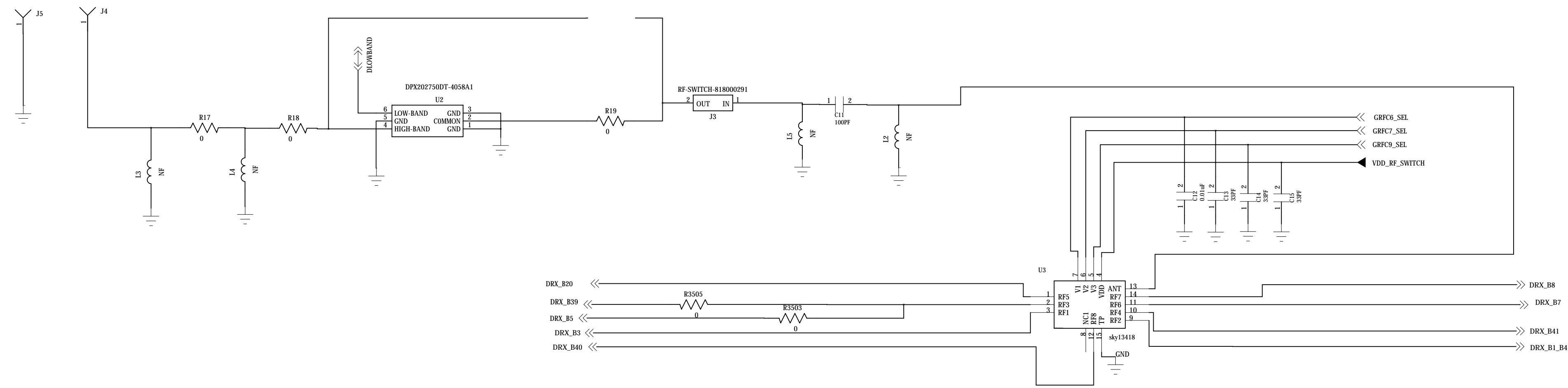


Band4041

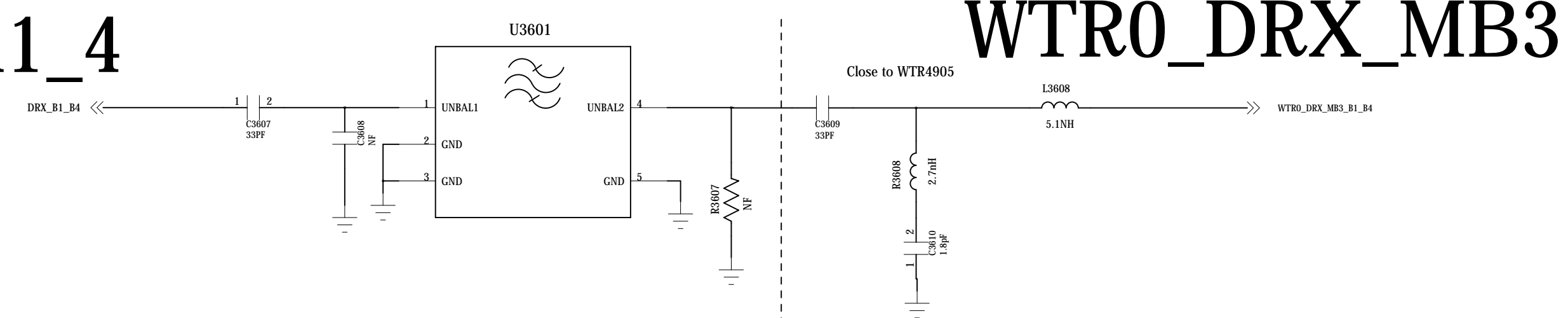


Note: The matching need close to WTR, RX ports have DC at the pin, so it need DC block,

Title	
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Size	Name
Disc:	Sheet of

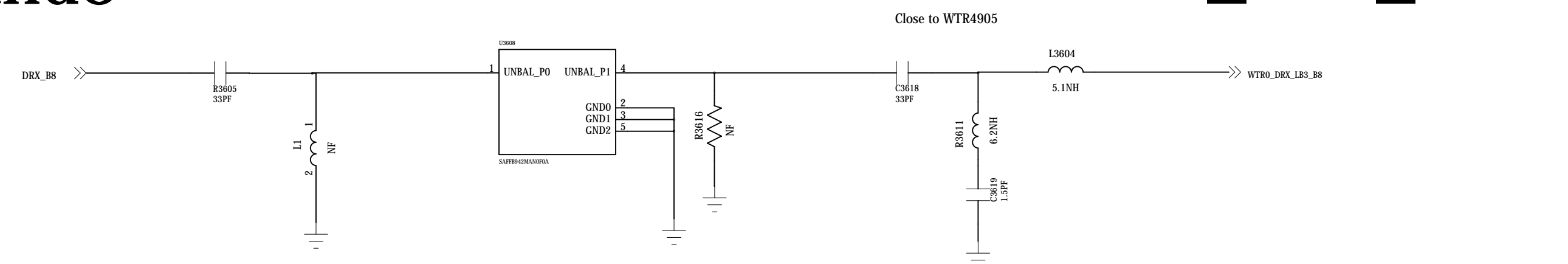


Band1_4



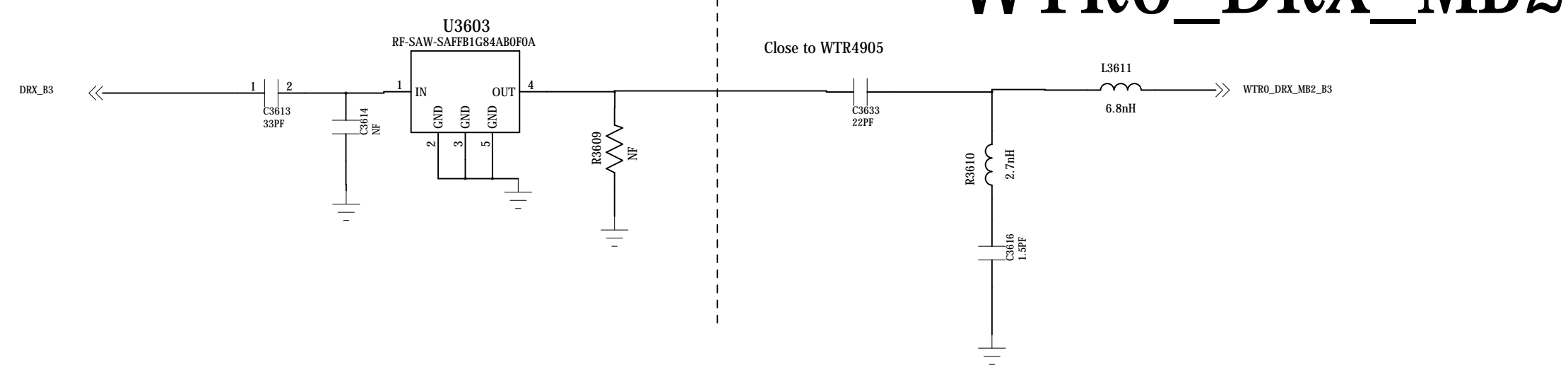
WTR0_DRX_MB3

Band8



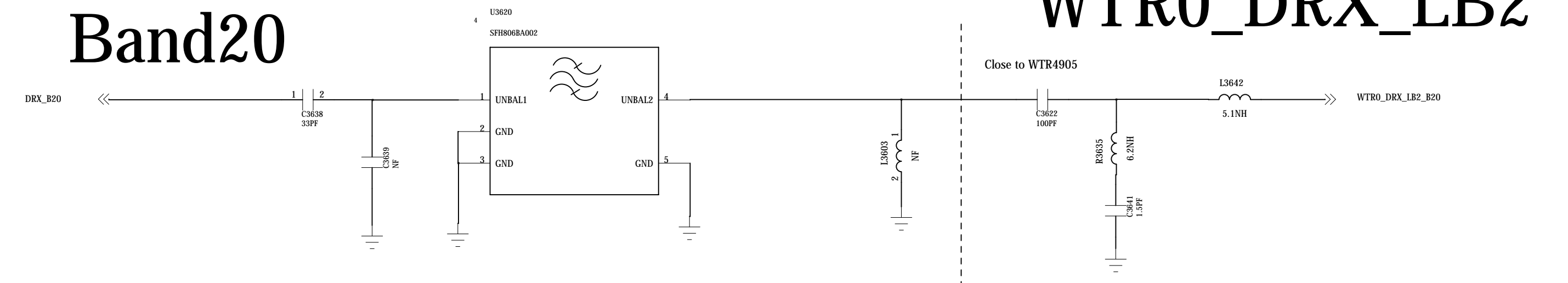
WTR0_DRX_LB3

Band3



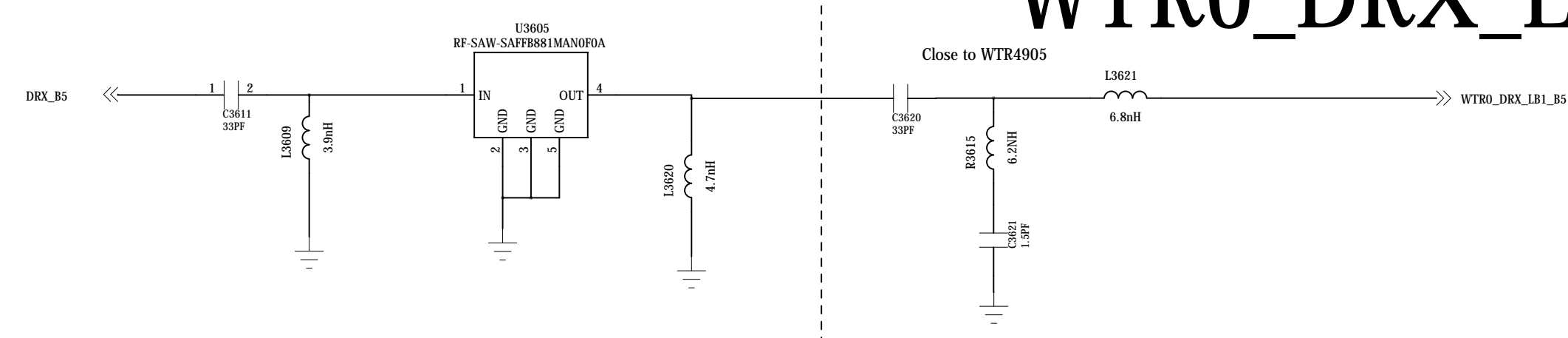
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Band20



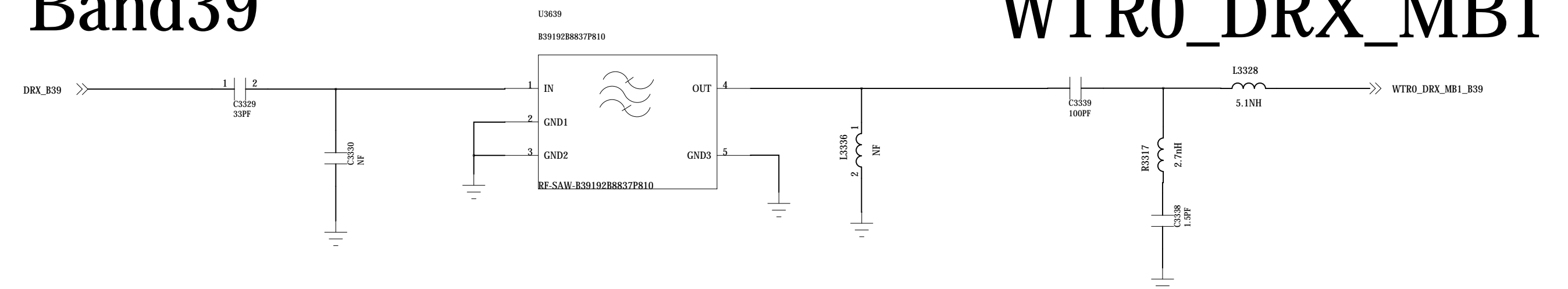
WTR0_DRX_LB2

Band5



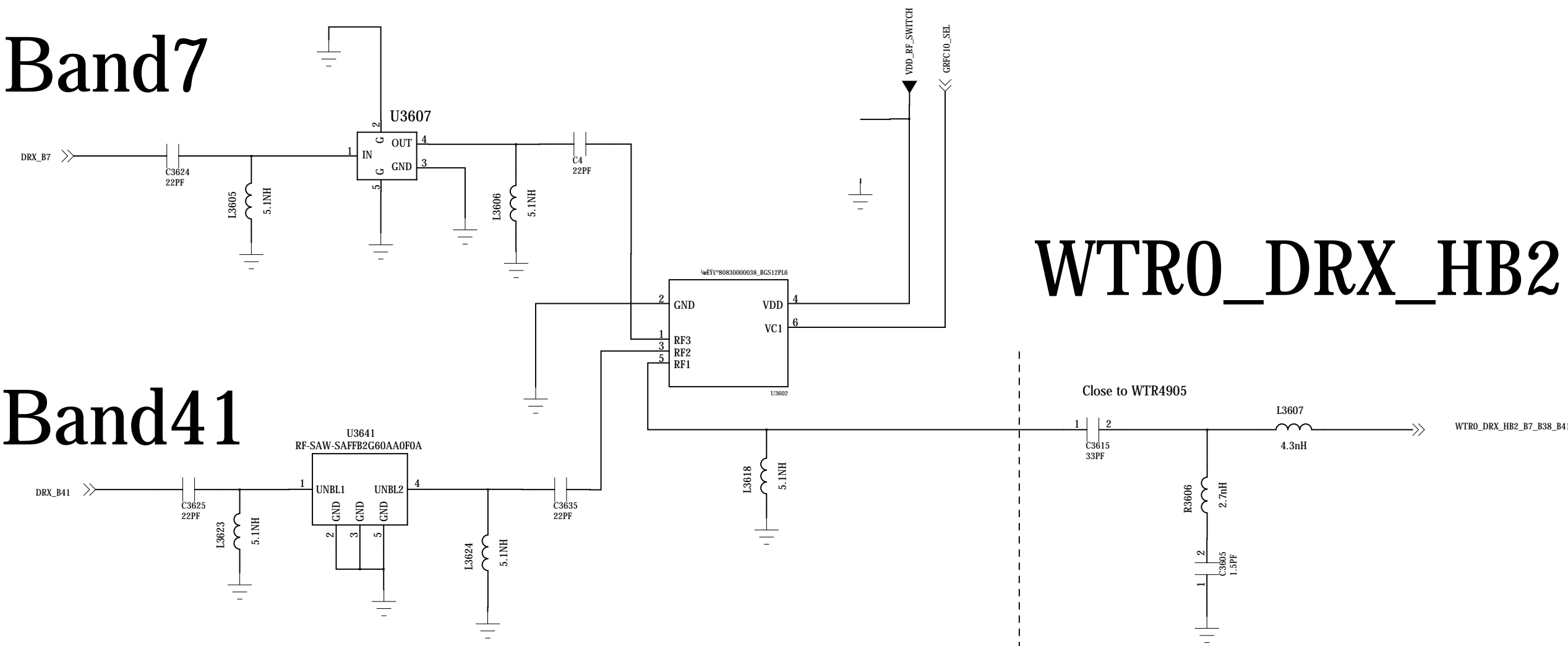
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Band39



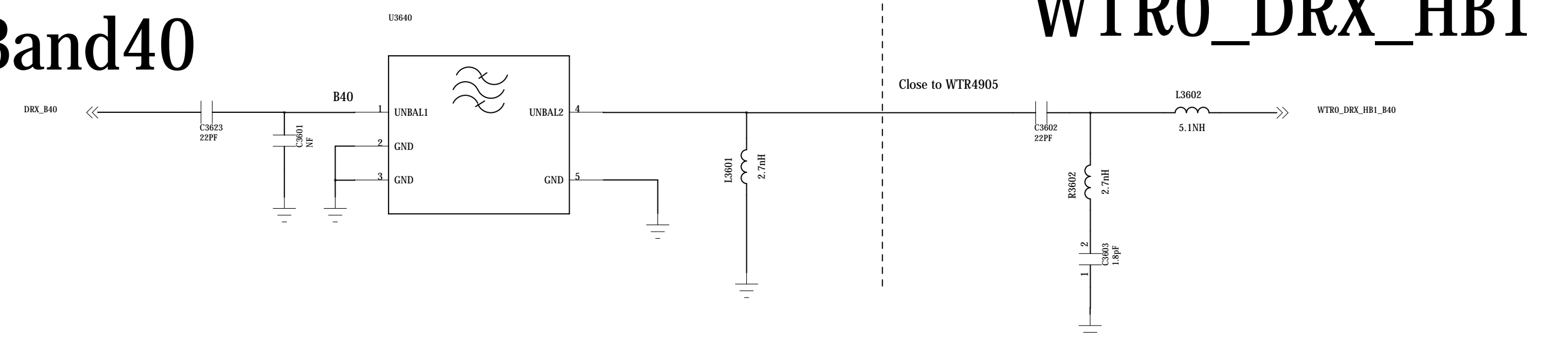
WTR0_DRX_MB1

Band7



WTR0_DRX_HB2

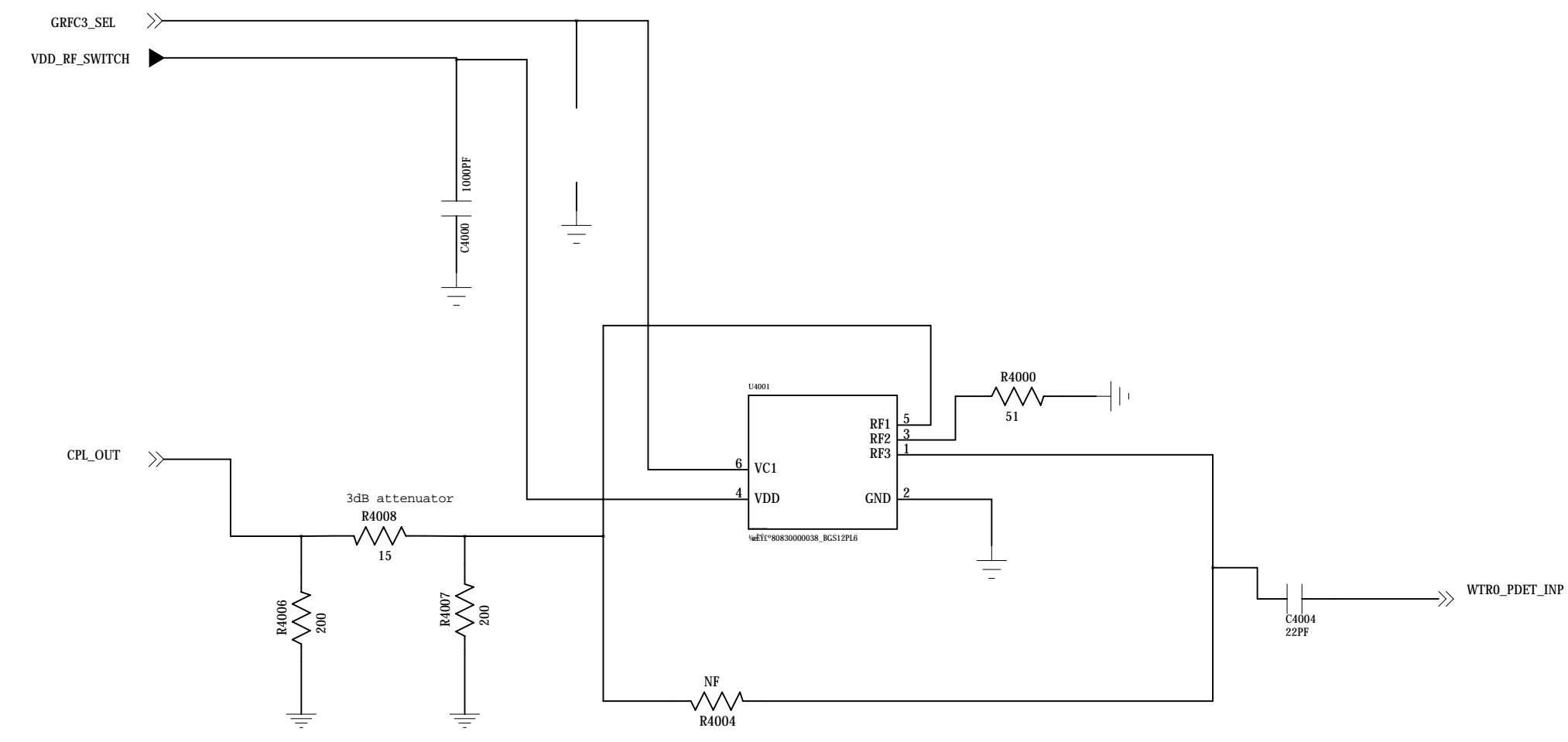
Band40



WTR0_DRX_HB1

Note: The matching need close to WTR, RX ports have DC at the pin, so it need DC block,

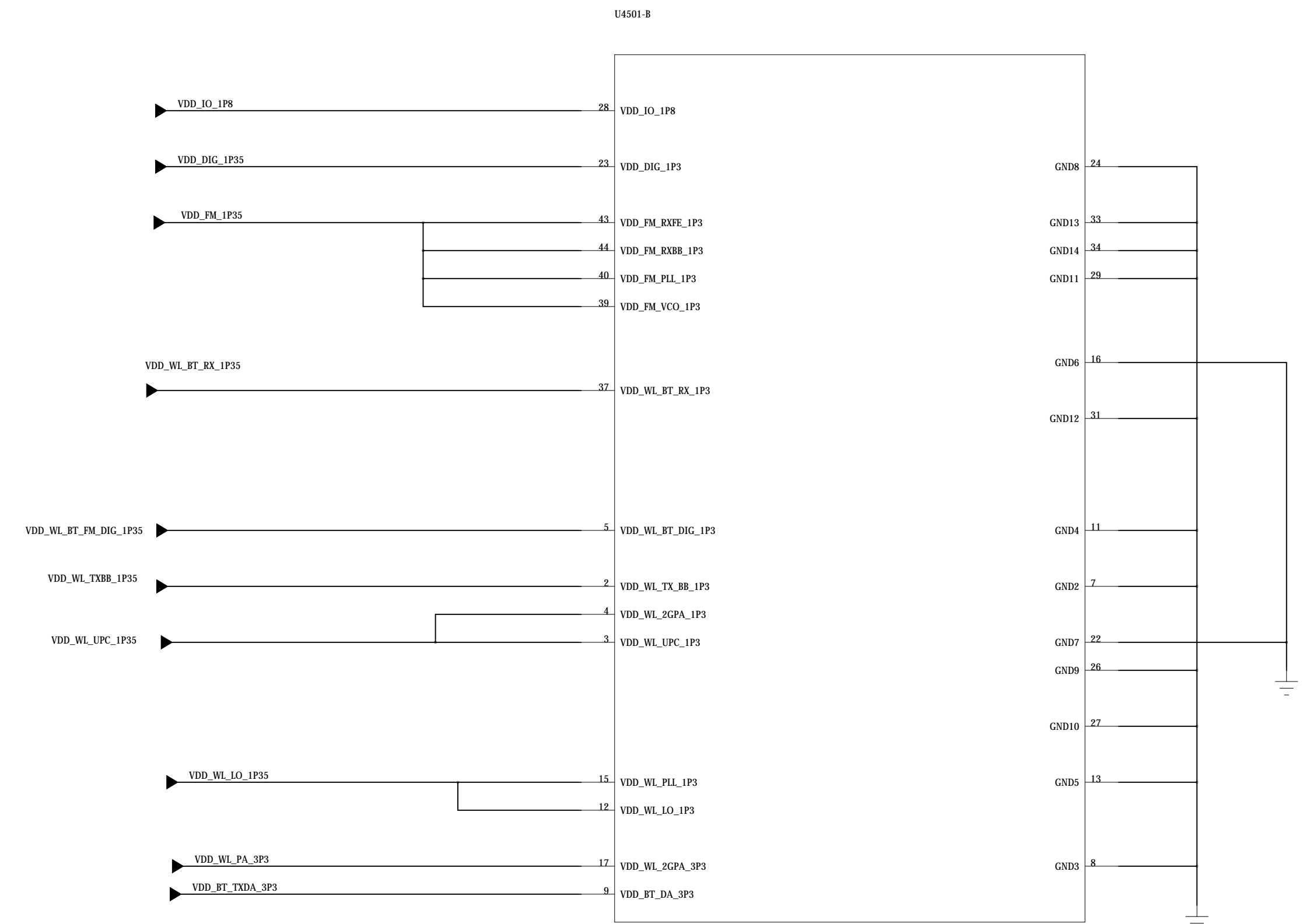
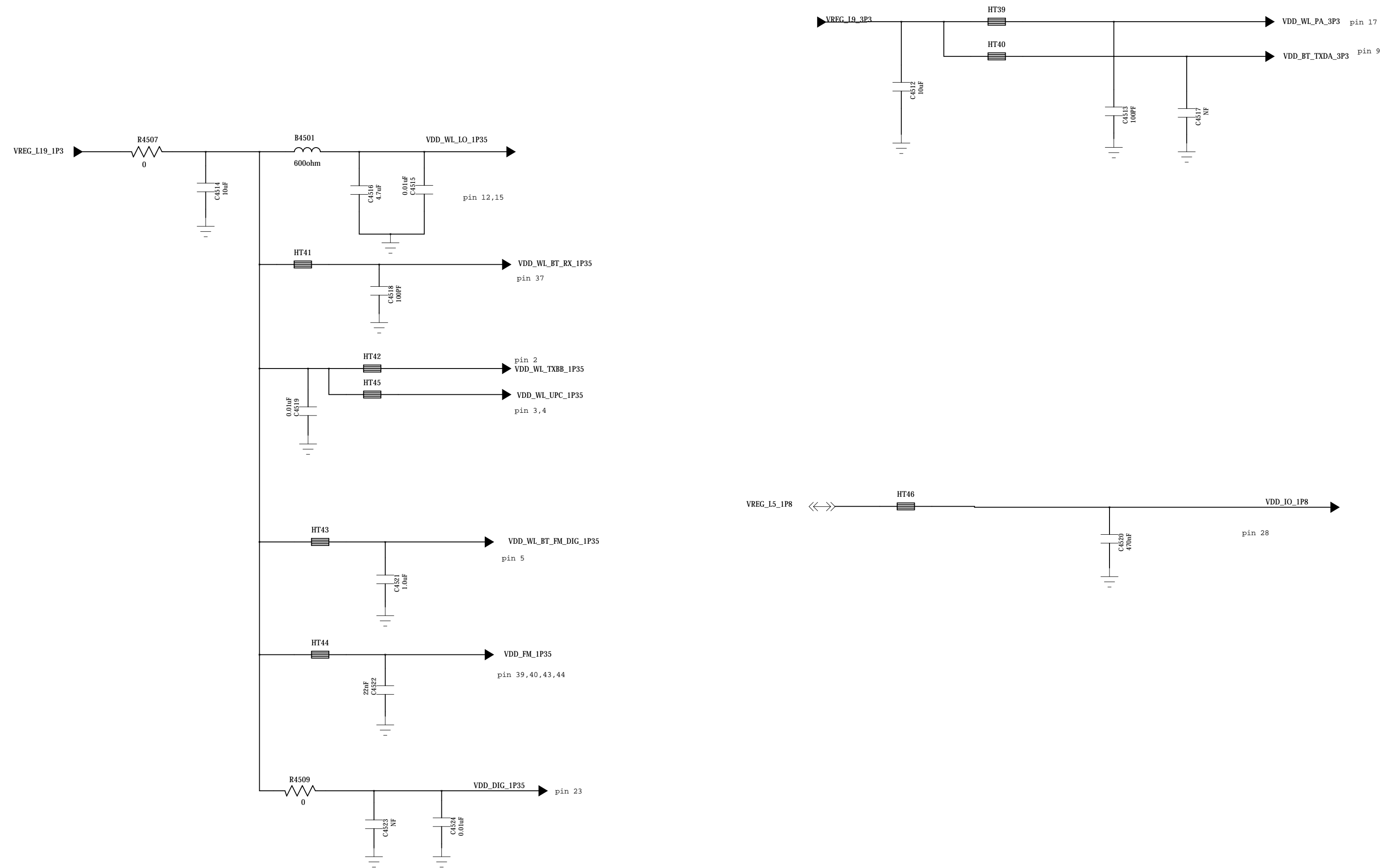
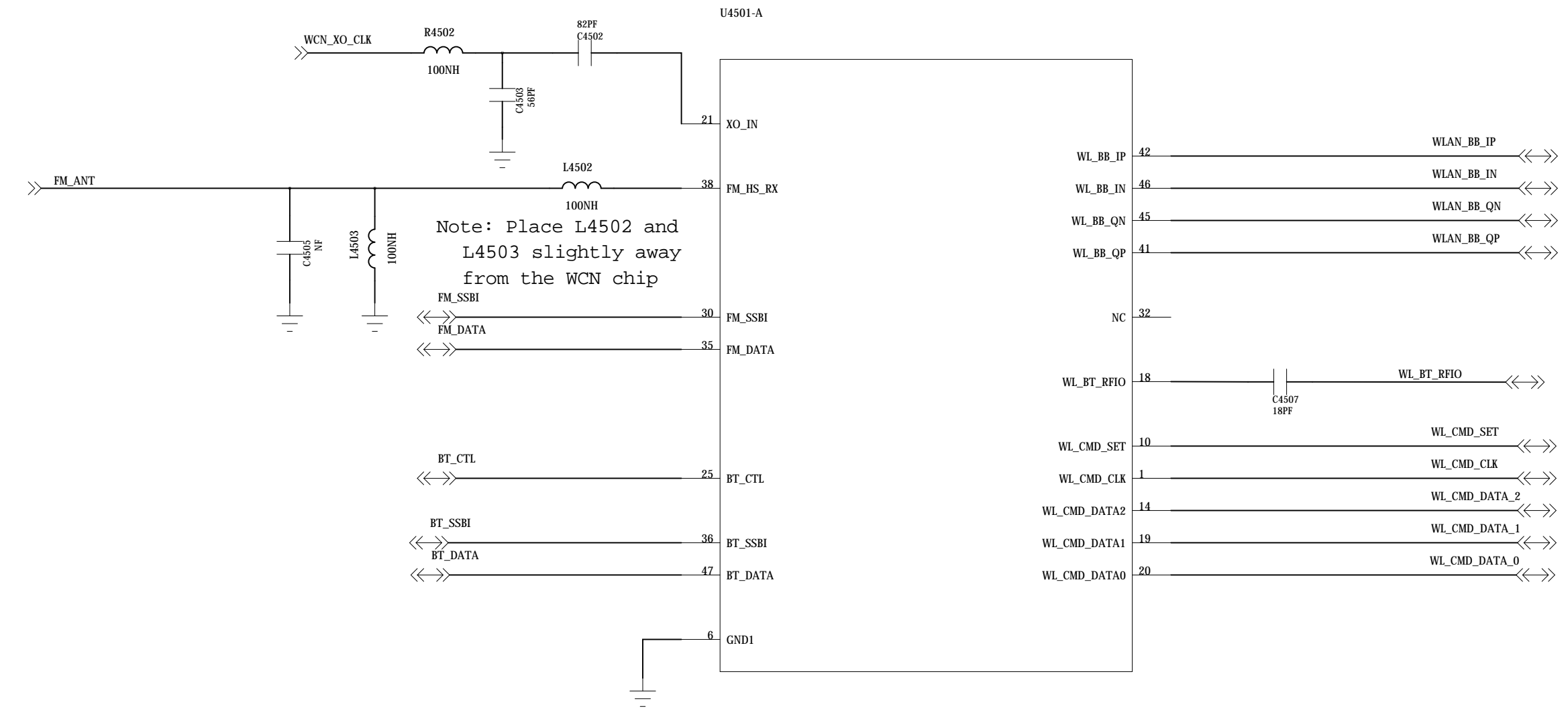
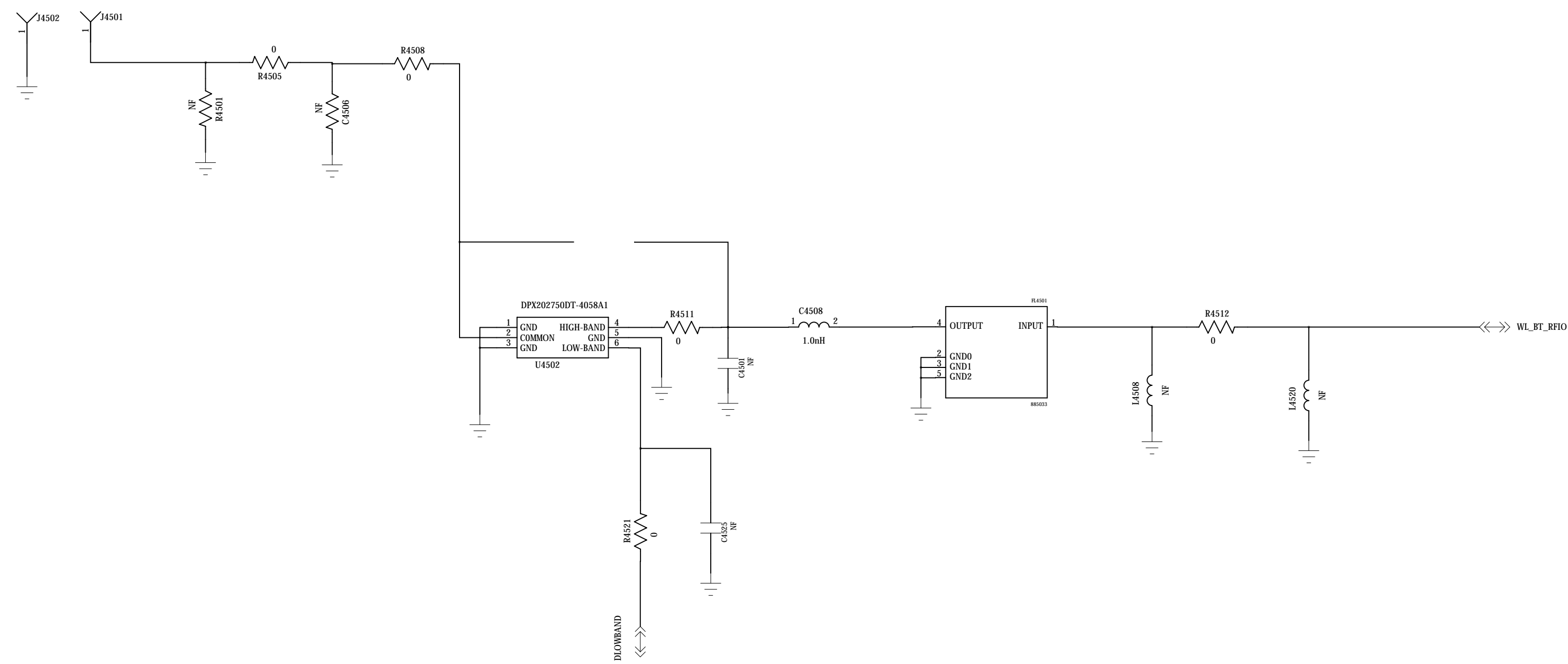
SPDT



Note: Use a single low impedance power plane/fill VPA for all ET PA VCC1/VCC2.

Refer to 80-NA681-91 rev.B or later revisions for more layout details.

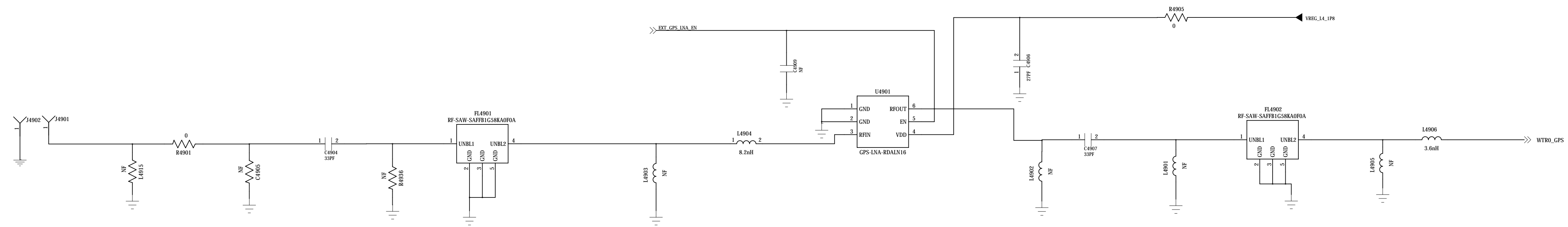
WCN



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San Diego, CA 92121-1714
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