A328 SERVICE MANUAL

V1.0

Documents statement:

- **This document is intended for use by qualified service personnel only.**
- **The documents only are used for service reference.**

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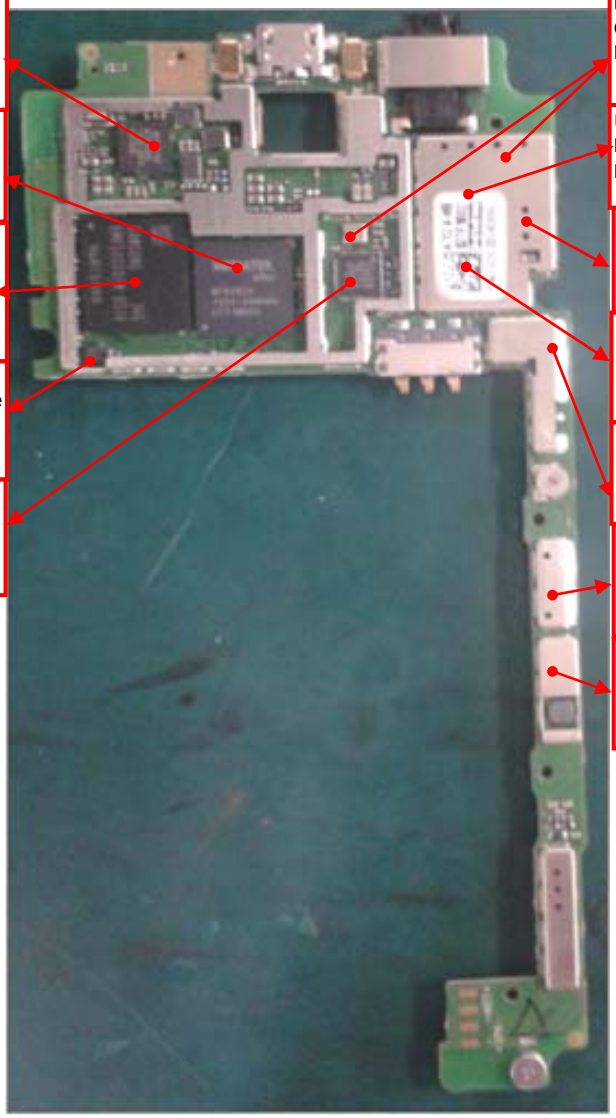
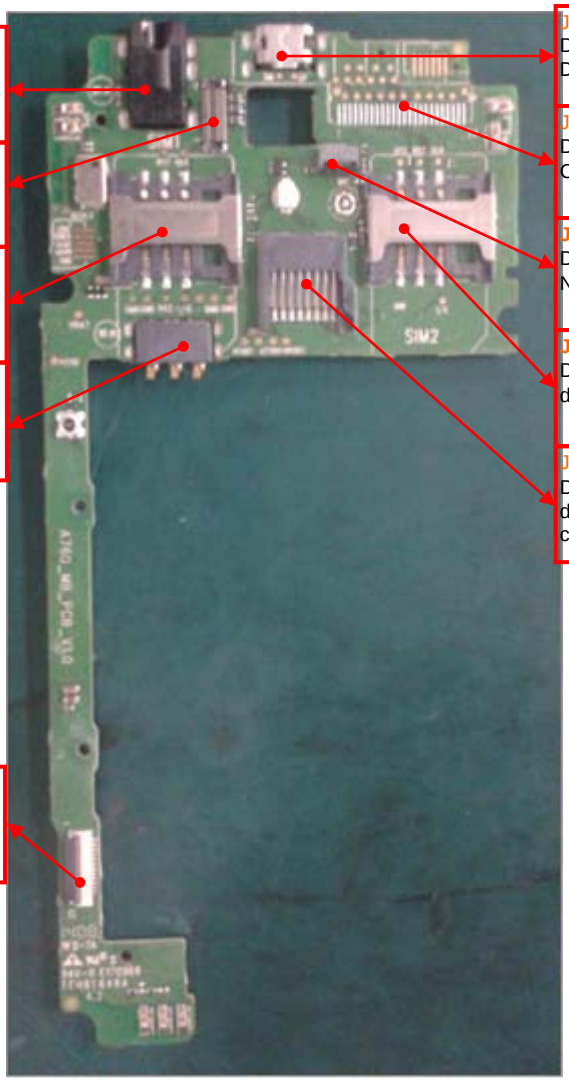
1. Product Figures

1-1. Exploded view





Part name

ITEM	Part No.	Model	QULITY
1	HQ11100239000	MT6582V/X	1
2	HQ11100133000	MT6166V	1
3	HQ11100242000	MT6323GA	1
4	HQ11110079000	MT6627N	1
5	HQ11120212000	5M39A46-5Z0//5M39A465Z0	1
6	HQ11160096000	VC5341	1
7	HQ11160115000	VC5348	1
8	HQ11150045000	ET5120A	1
9	HQ11220005000	WPT2N41-8/TR	1
10	HQ11180029000	BMA223	1

1-2. Product Main Function

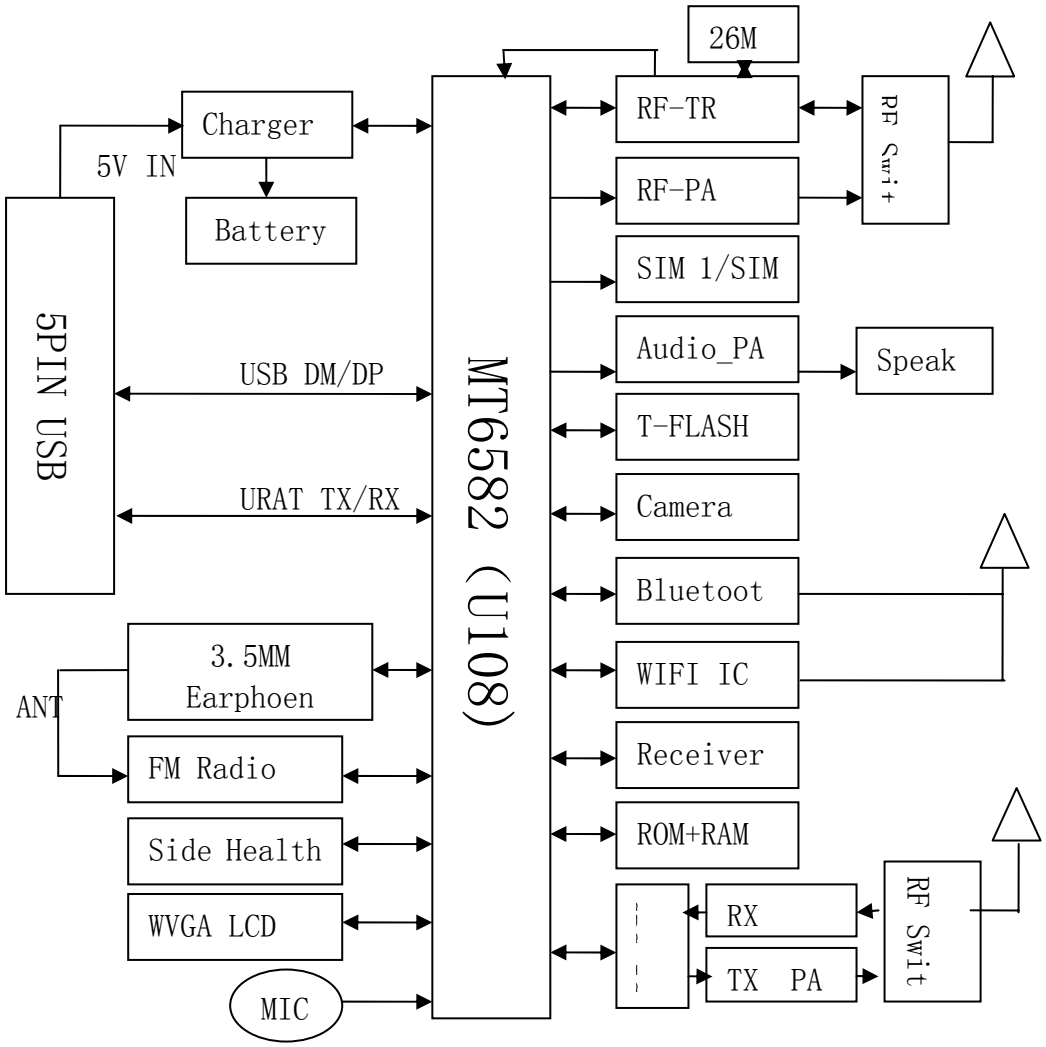
- Support Camera
- Music player
- Support T-Flash card
- Support WIFI
- 4.0" WVGA LCD
- Support GSM850&GSM900&DCS1800&PCS1900&WCDMA900&WCDMA2100 Network
- Support Bluetooth
- Support FM radio
- Support dual SIM card
- Support G-sensor
- Support GPS

1-3. General Specificatio

	EGSM 900 Phase 2	DCS1800 Phase 1	PCS1900
Freq. Band[MHz] Uplink/Downlink	880~915 925~960	1710~1785 1805~1880	1850～1910 1930～1990
ARFCN range	0~124 & 975~1023	512~885	512~810
Tx/Rx spacing	45 MHz	95 MHz	80 MHz
Mod. Bit rate/ Bit Period	270.833 kbps 3.692 us	270.833 kbps 3.692 us	270.833 kbps 3.692 us
Time Slot Period/Frame Period	576.9 us 4.615 ms	576.9 us 4.615 ms	576.9 us 4.615 ms
Modulation	0.3 GMSK	0.3 GMSK	0.3 GMSK
MS Power	33 dBm~5 dBm	30 dBm~0 dBm	30 dbm～0 dbm
Power Class	5 pcl ~ 19 pcl	0 pcl ~ 15 pcl	0 pcl~15 pcl
Sensitivity	-102 dBm	-100 dBm	-100 dbm
TDMA Mux	8	8	8

2. Block Diagrams

2-1. System Diagrams



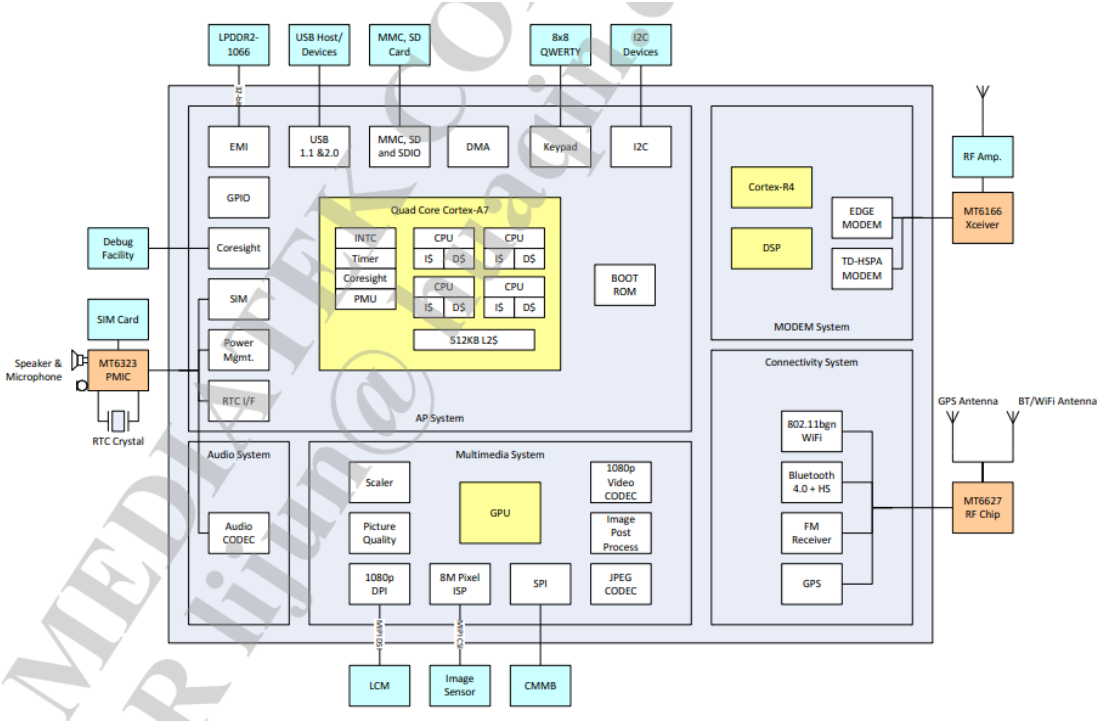
Remark: FM/GPS/WIFI/BT to Four in Chip;

2-1-1 BBIC Diagrams

MediaTek MT6572 is based on four core ARM architecture (28nm A7 architecture) ,frequency of 1.3 GHz,can be seen MT6572 quad-core upgraded or modified MT6589 , in addition the GPU or the first TD-SCDMA and WCDMA dual-mode integrated in the same single chip(can be seen as MTK6582 will bring TD baseband chips ,the disputed).At the same time ,mediatek will also launch MT6582M Mt6582 cheap version . Including mediatek MT6582 highest level support 720P resolution screen ; Mediatek Mt6582 is the highest level can only support the QHD screen .Frequency is 1.3GHz,collocation of

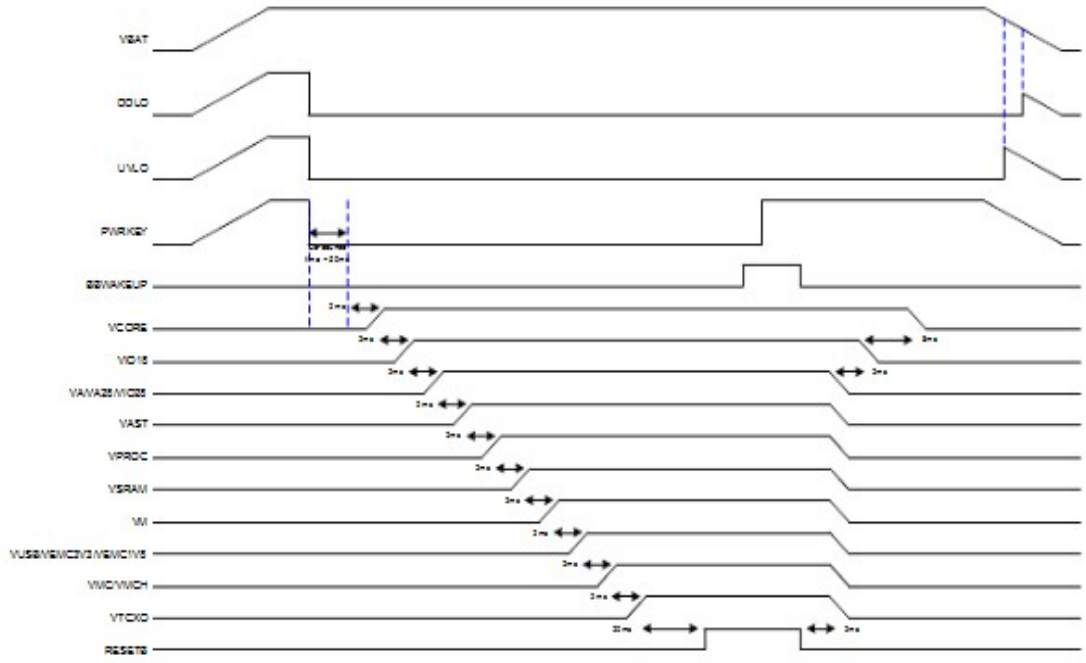
GPU models for SGX still 544.

Typical application diagram is shown in nether figure



Application Diagram of MT6582

2-2. Power Management Diagrams



	Symbol	Vout (V)	Iout (mA)
Buck	VPA	0.9 ~ 3.4 (100mV/step)	800
	VPROC	0.75 ~ 1.3 (25mV/step)	1500
	VRF18	1.825	250
	VCORE	0.75 ~ 1.3 (25mV/step)	1000
	VIO18	1.8	1000
Analog LDO	VRF28	2.85	200
	VTCXO	2.8	40
	VCAMA	1.5/1.8/2.5/2.8	200
Digital LDO	VA1	1.8/2.0/2.1/2.5	100
	VA2	2.5/2.8	100
	VM12_1	1.2	300
	VM12_2	1.2	300
	VM12_INT	1.2	300
	VIO28	2.8	100
	VSIM1	1.8/3.0	100
	VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VUSB	3.3	100
	VCAMD	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	300
	VCAM_IO	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VCAM_AF	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200
	VMC	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200
	VMCH	1.3/1.5/1.8/2.5/2.8/3.0/3.3	400
	VGP	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
	VGP2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100
Vibrator	VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200
RTC	VRTC	1.8/2.0/2.1/2.8	2

3. Flow Chart of Troubleshooting

3-1.Baseband

3-1-1. Phone does not start up troubleshooting

Power-on Sequence and Protection Logic:

The PMU handles the powering ON and OFF of the handset. There are three ways to power-on the handset system :

① Push PWRKEY (Pull the PWRKEY pin to the low level)
② RTC module generate PWRBB to wakeup the system
③ Valid charger plug-in (CHRIN voltage is within the valid range)

Pulling PWRKEY low is the typical way to turn on the handset. The Vcore buck converter will be turned-on first, and then Va/Vio/Vm LDOs turn-on at the same time. After that, the supplies for the baseband are ready and it will send the PWRBB signal back to PMU for acknowledgement. To successfully power-on the handset, PWRKEY should be kept low until PMU receives the PWRBB from BB. Besides, the system reset ends at the moment when the Vcore/Va/Vio/Vm are fully turned-on to ensure the correct timing and function.

If the RTC module is scheduled to wakeup the handset at some time, the PWRBB signal will directly control the PMU. In this case, PWRBB becomes high at the specific moment and let PMU power-on just like the on-sequence described above. This is the case named RTC alarm.

Charger plugging-in will also turn on the handset if the charger is a valid charger. However, if the battery voltage is too low to power-on the handset (UVLO state), the system won't be turned-on by any of the three ways. In this case, charger will charge the battery first and the handset will be powered-on automatically as long as the battery voltage is high enough.

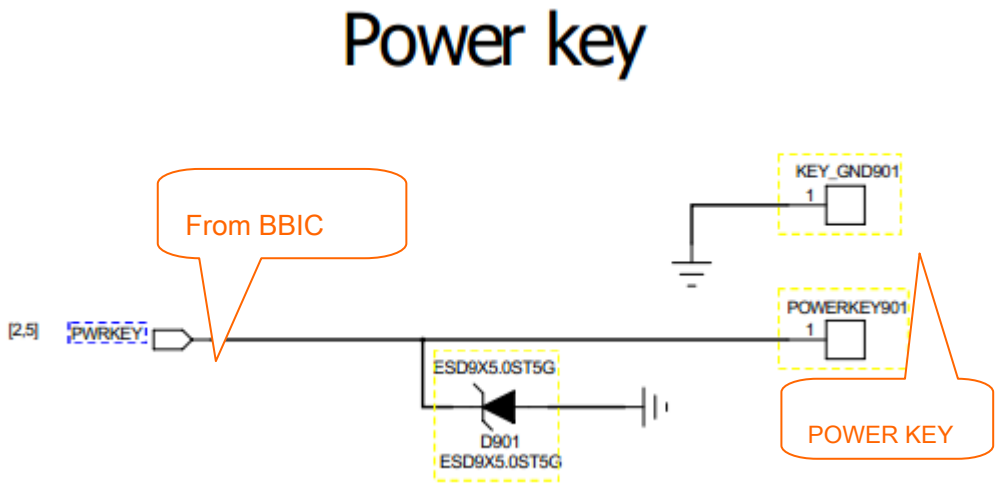
States of mobile handset and regulator

Phone State	CHRON	UVLO	PWRKEY && (~PWRBB)	Vrtc (1st step)	Vcore, Vio, Vm, Va	Vtcxo, Vrf
No Battery or Vbat < 2.5V	X	H	X	Off	Off	Off
2.5V < Vbat < 3.2V	L	H	X	On	Off	Off
Pre-Charging	H	H	X	On	Off	Off
Charger-on (Vbat>3.2V)	H	L	X	On	On	On
Switched off	L	L	H	On	Off	Off
Stand-by	L	L	L	On	On	Off
Active	L	L	L	On	On	On

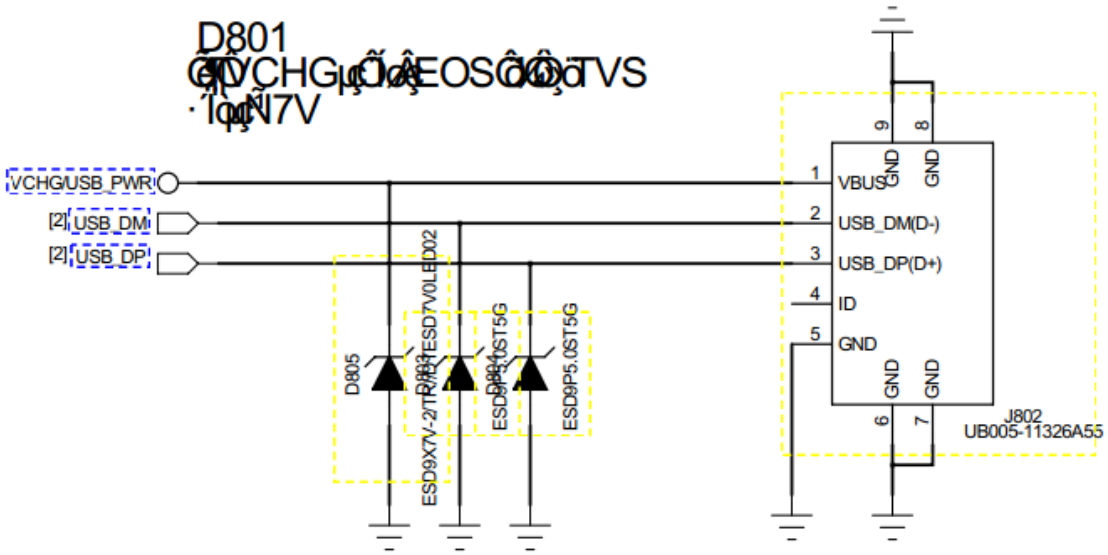
Troubleshooting flow chart

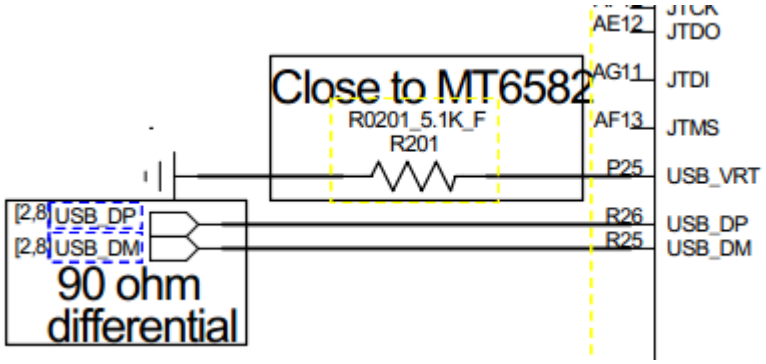
Main related component: BBIC(U108) , NAND+SDRAM(U401), XTAL CRYSTAL (X101),RF-TR(U201), PMIC (U501) ,Power button.

Power ON/OFF and download circuit



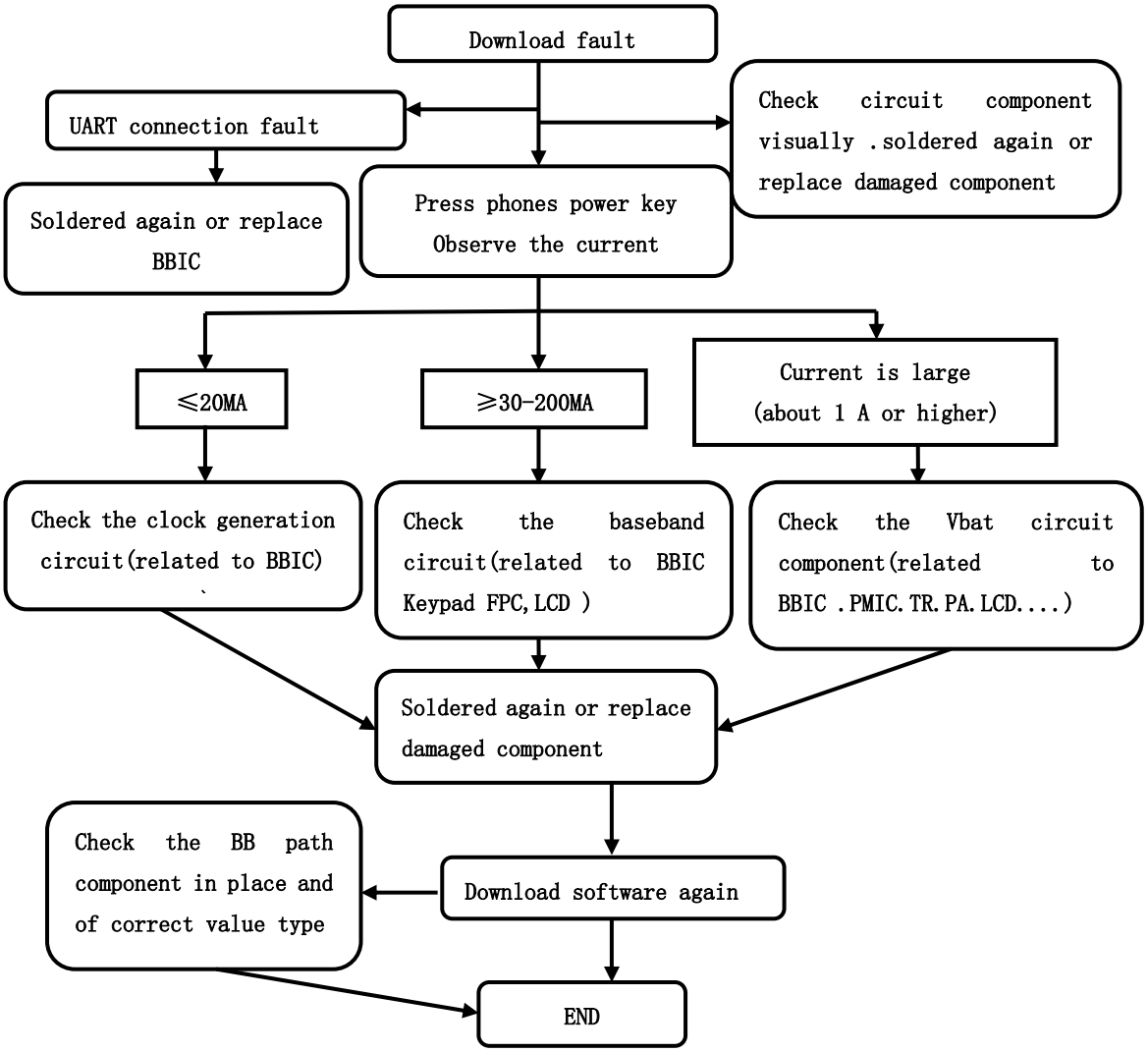
- MINI USB CIRCUIT





Download troubleshooting

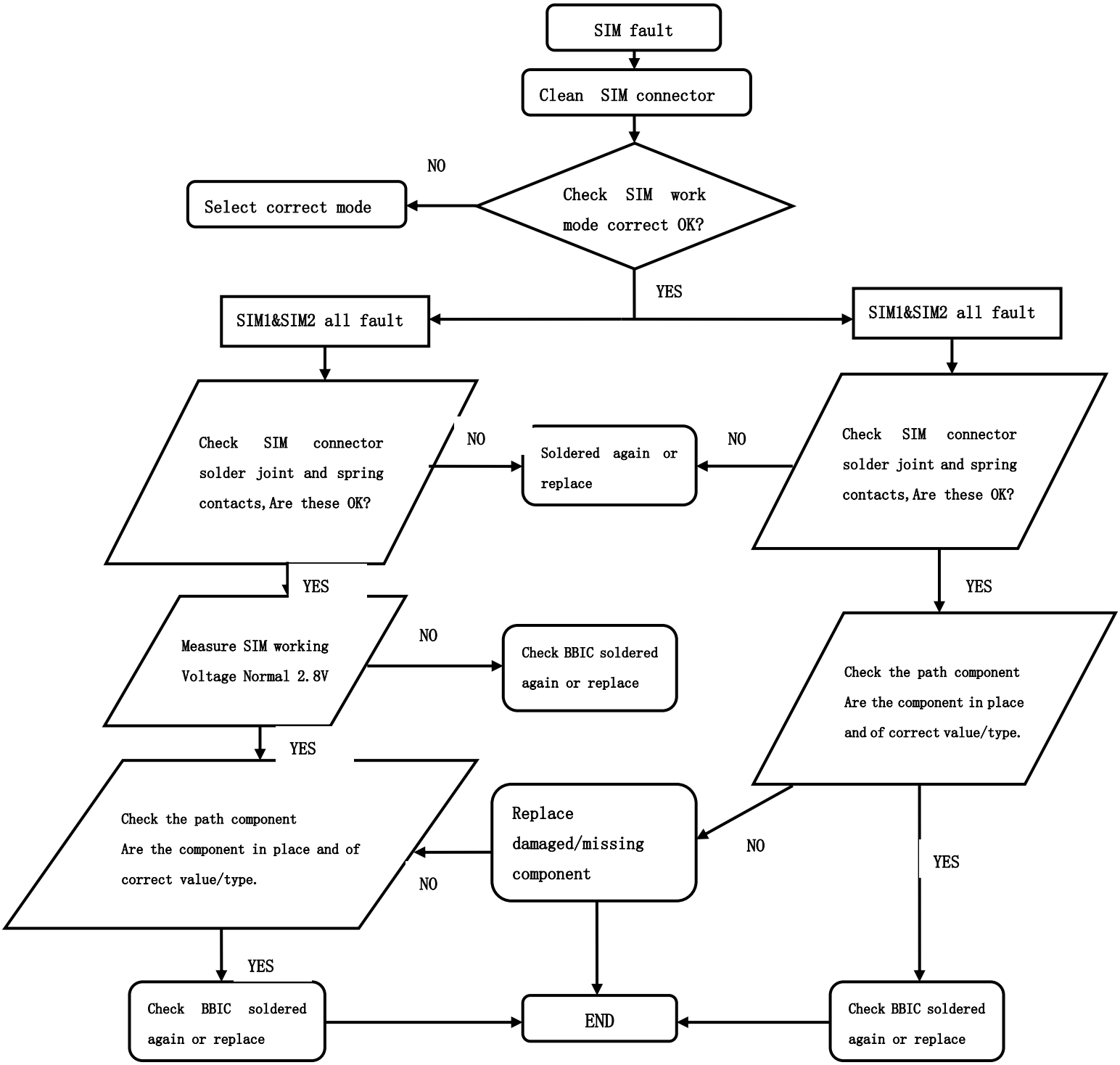
Main related component: BBIC(U108) , NAND+SDRAM(U401),RF-TR(U106), XTAL CRYSTAL (X101) , MINI USB(J802).



3-1-2. SIM troubleshooting

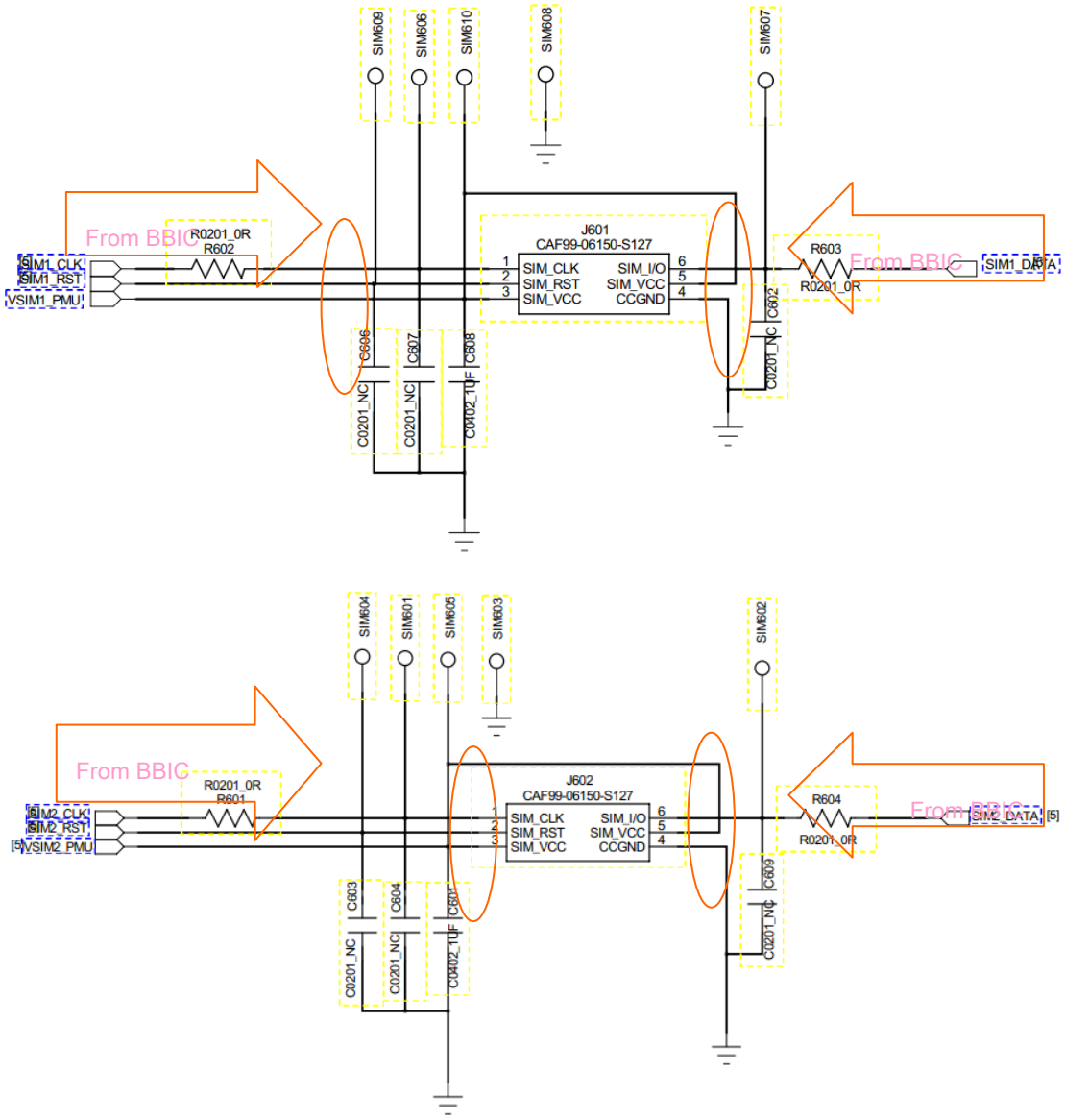
Troubleshooting flow chart

Main related component: BBIC(U108), SIM connector(J601,J602)



SIM CIRCUIT

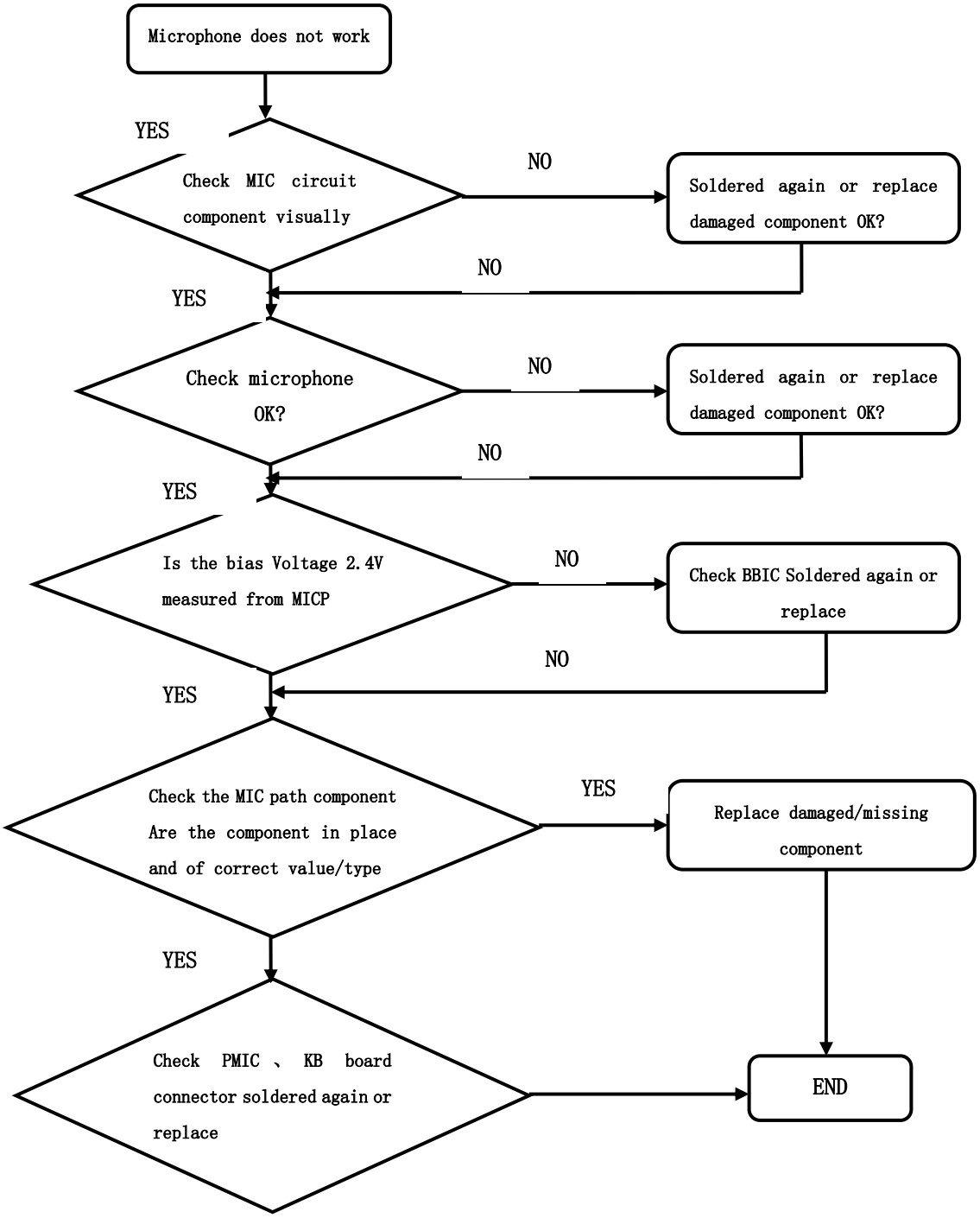
- SIM1&SIM2



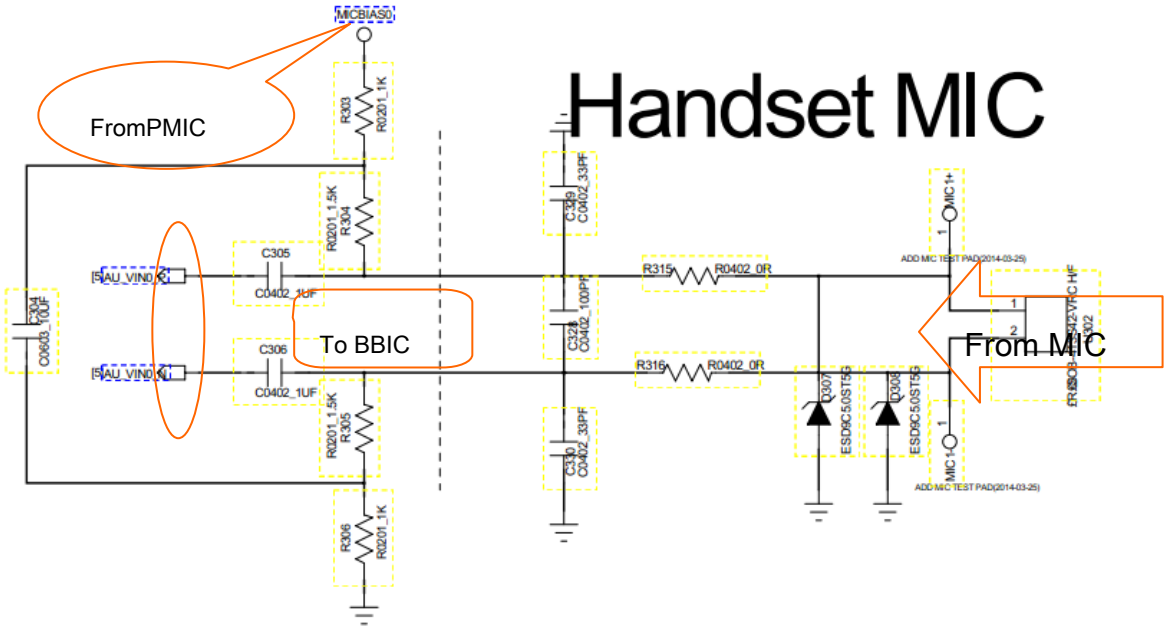
3-1-3. MIC troubleshooting

Troubleshooting flow chart

Main related component: BBIC(U108),MIC



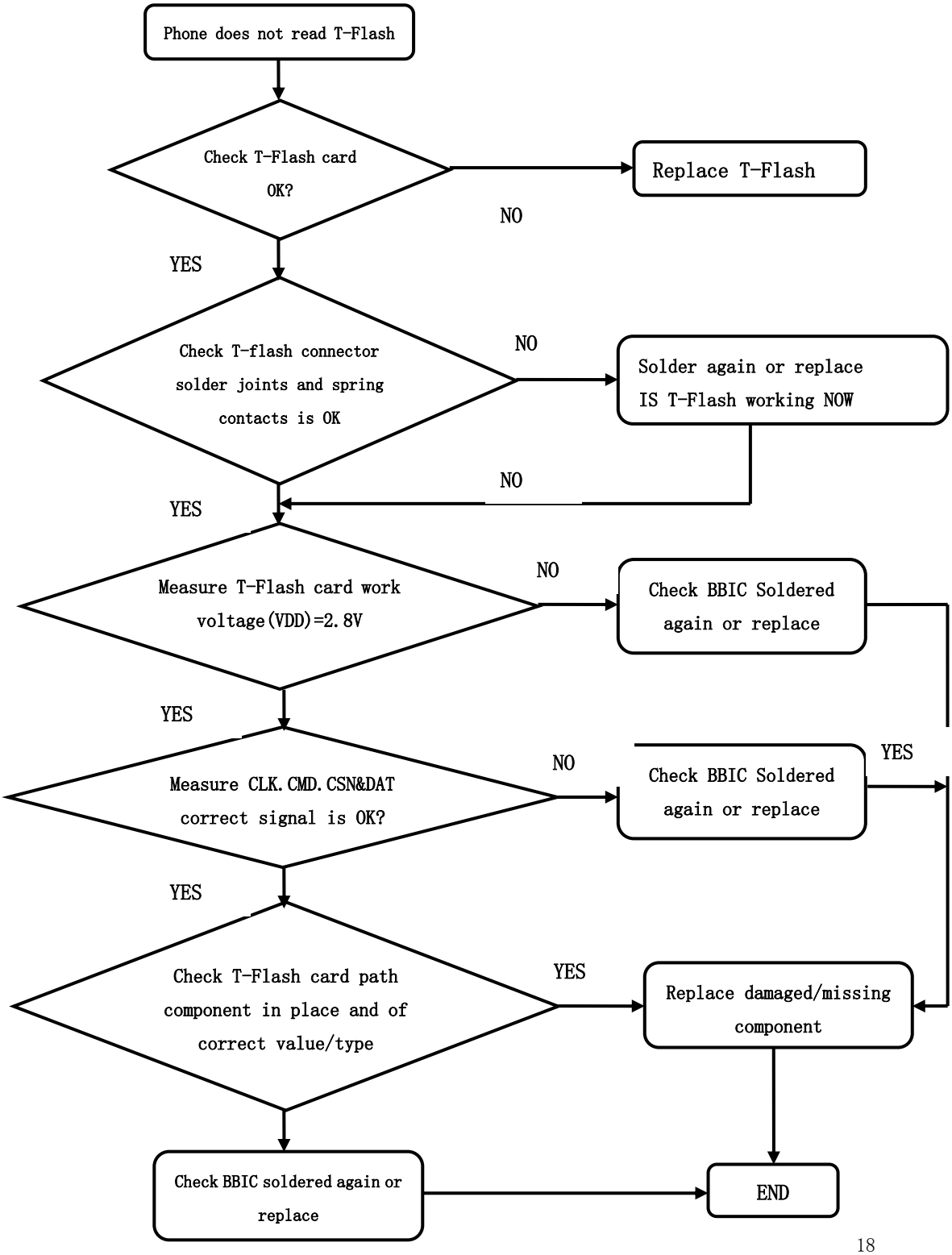
MIC circuit



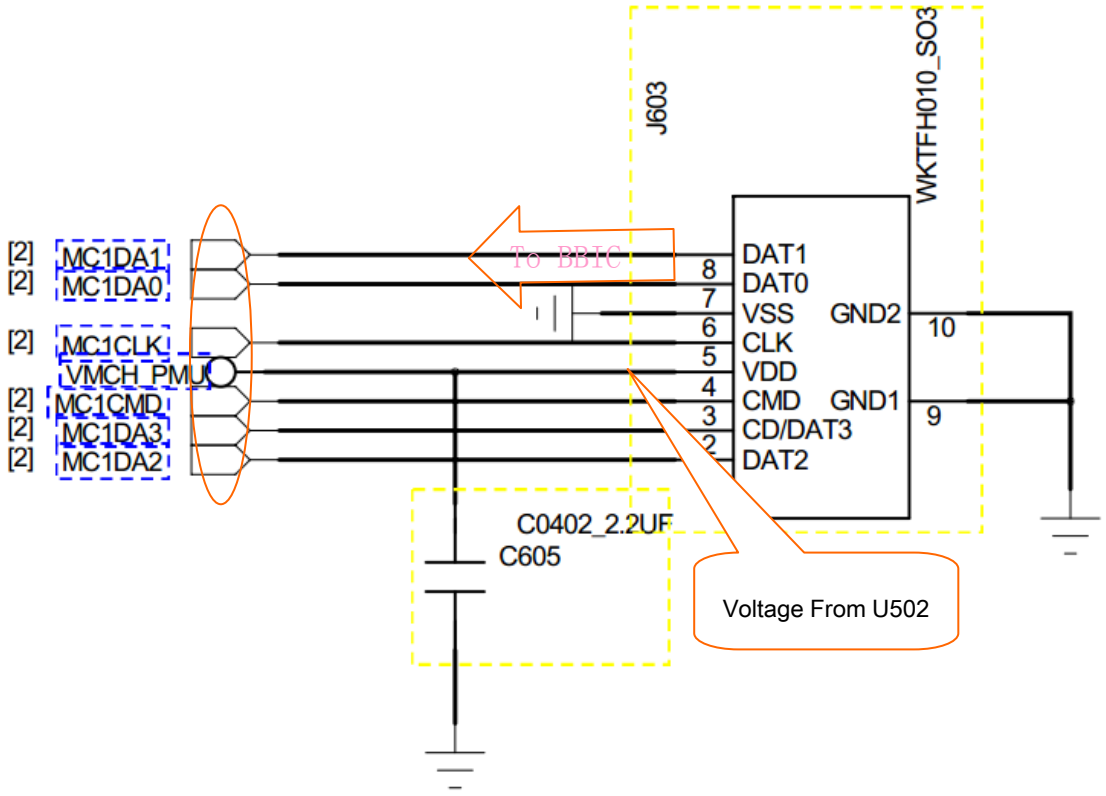
3-1-4. T-Flash troubleshooting

Troubleshooting flow chart

Main related component: BBIC(U108)，T-FLASH CONNECTOR(J603).

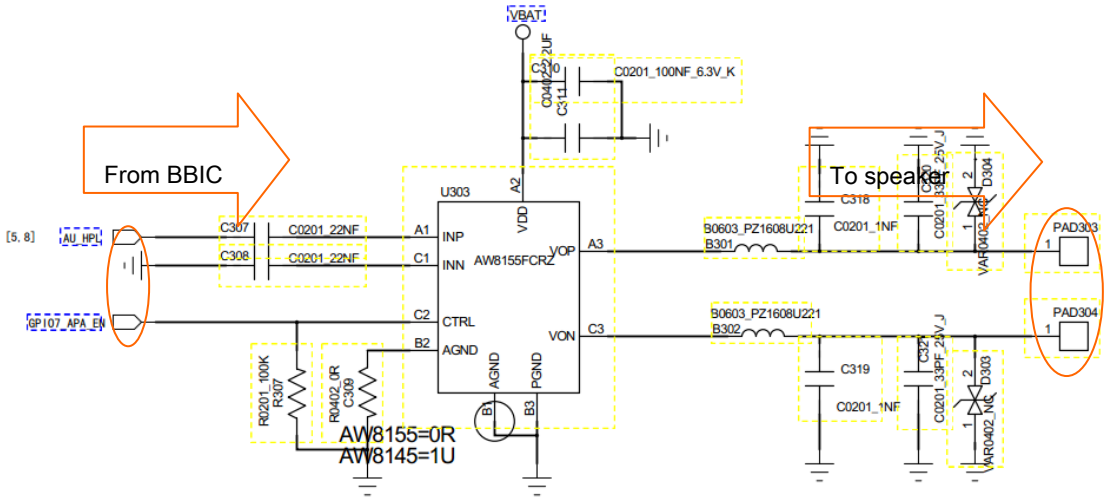


T-Flash circuit



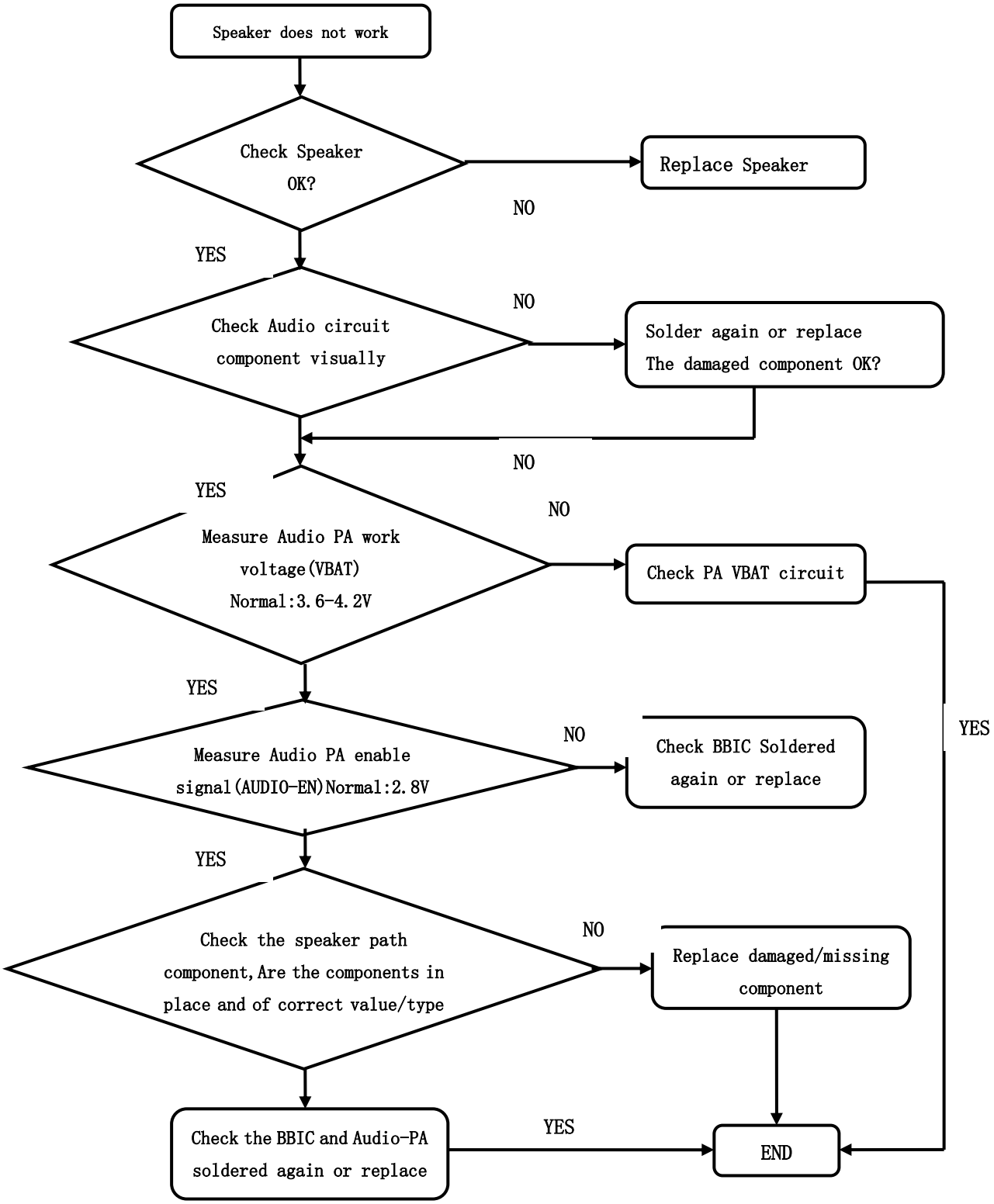
3-1-5. Speaker troubleshooting

Speaker circuit



Troubleshooting flow chart

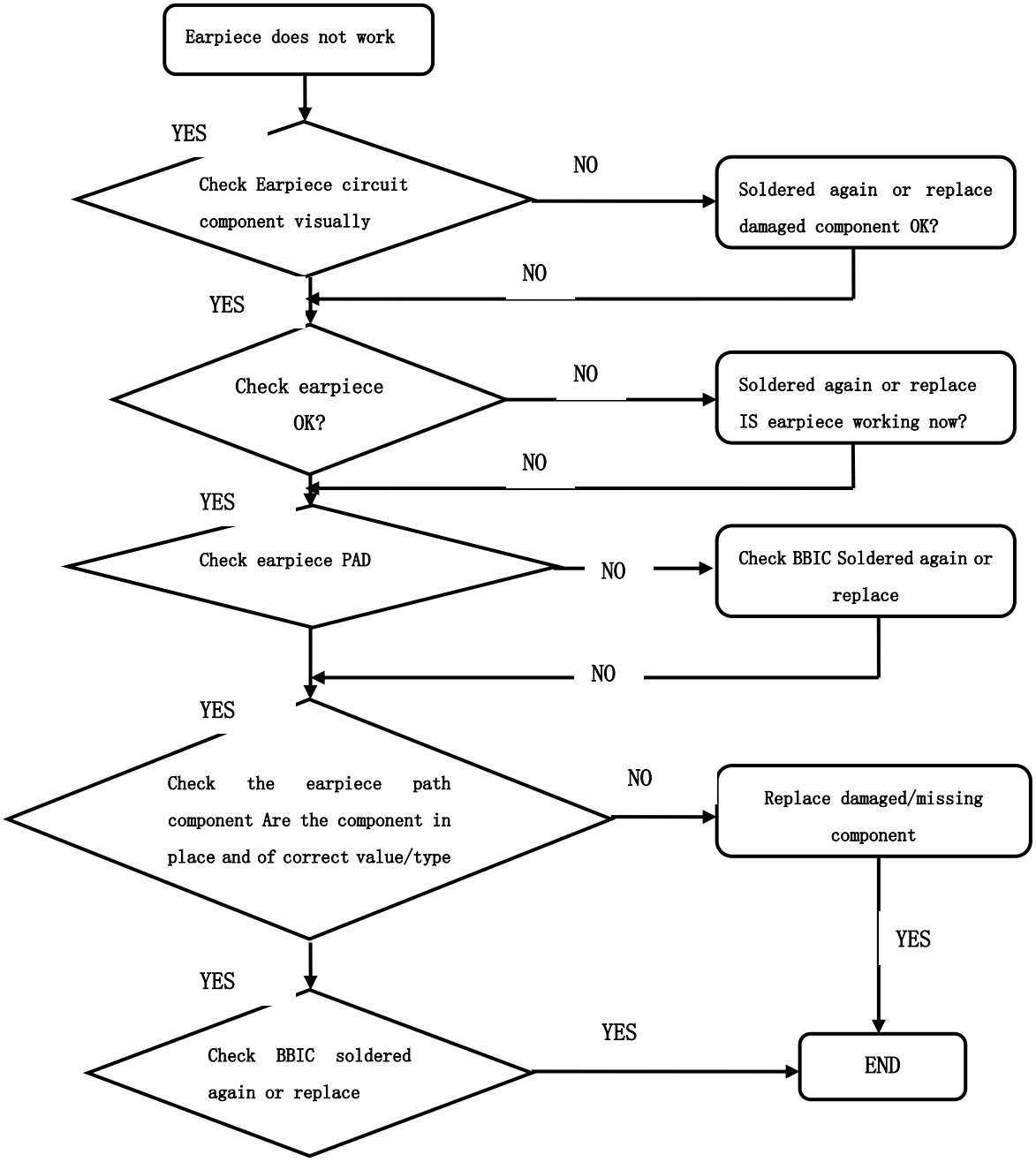
Main related component: BBIC(U108),SPEAKER



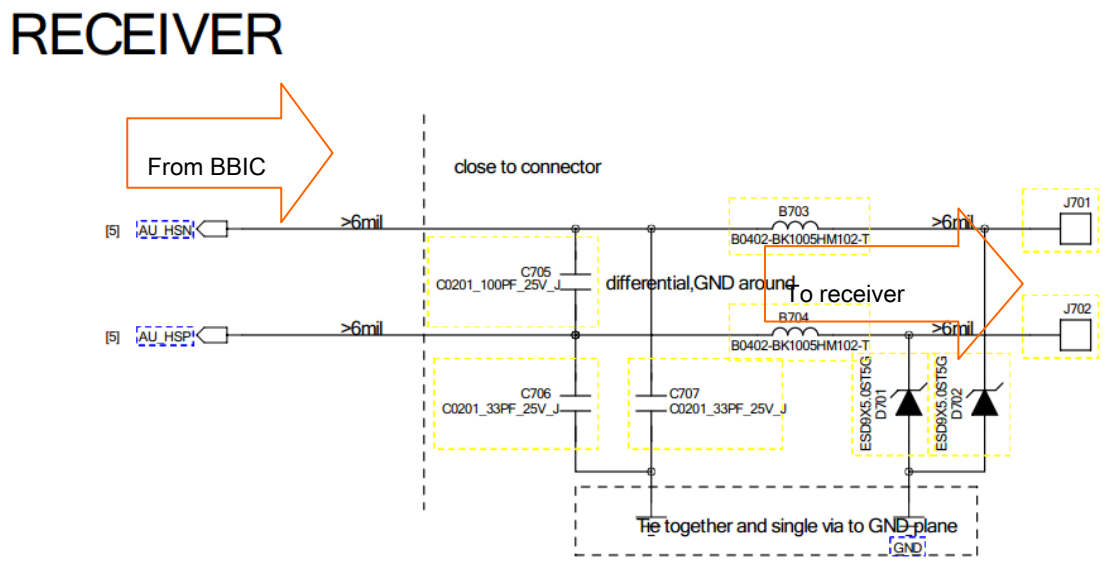
3-1-6. Receiver troubleshooting

Troubleshooting flow chart

Main related component: BBIC(U108),Receiver



Receiver circuit

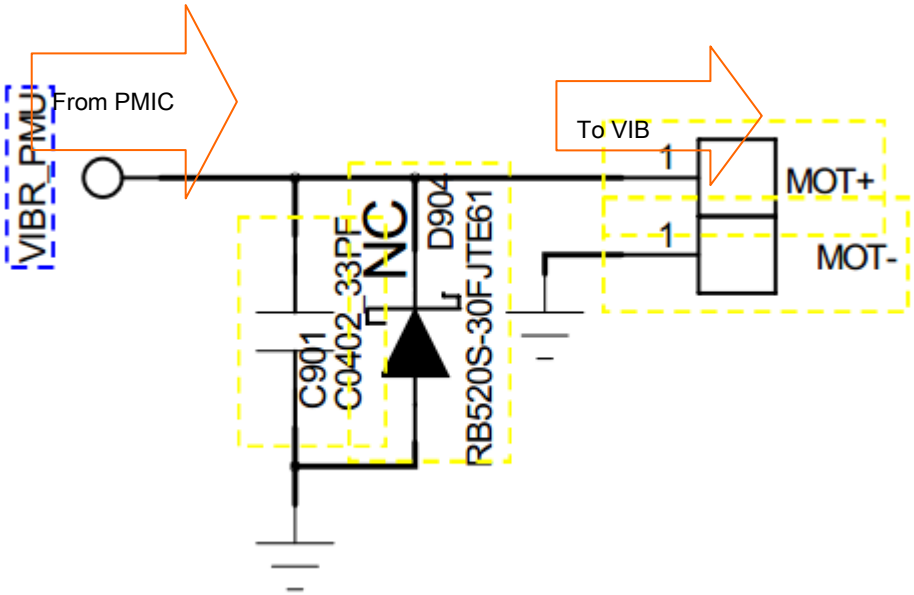


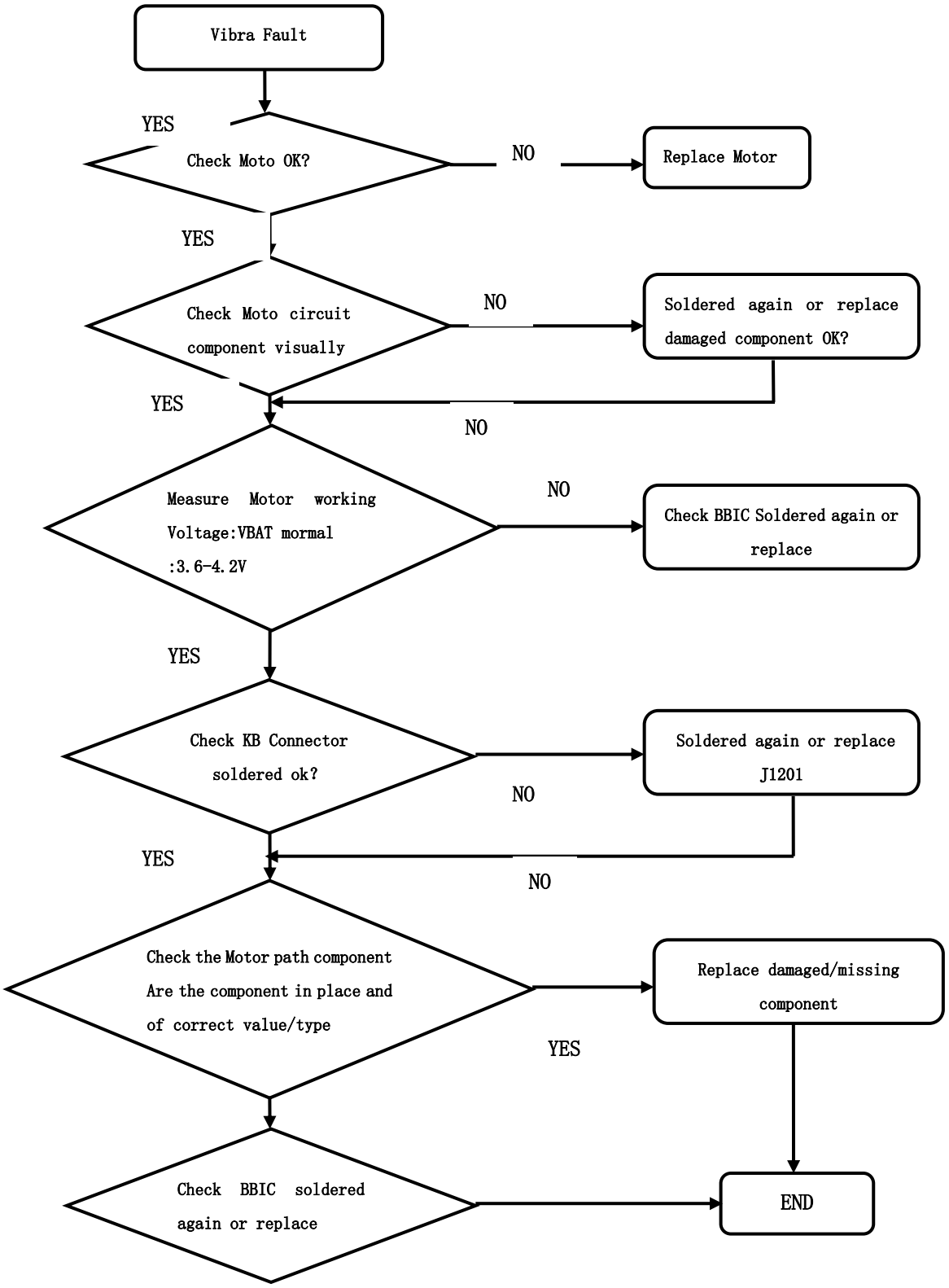
3-1-7. Vibra troubleshooting

Troubleshooting flow chart

Main related component: BBIC,MOTOR , KB board ConnectorJ1201

Vibra circuit

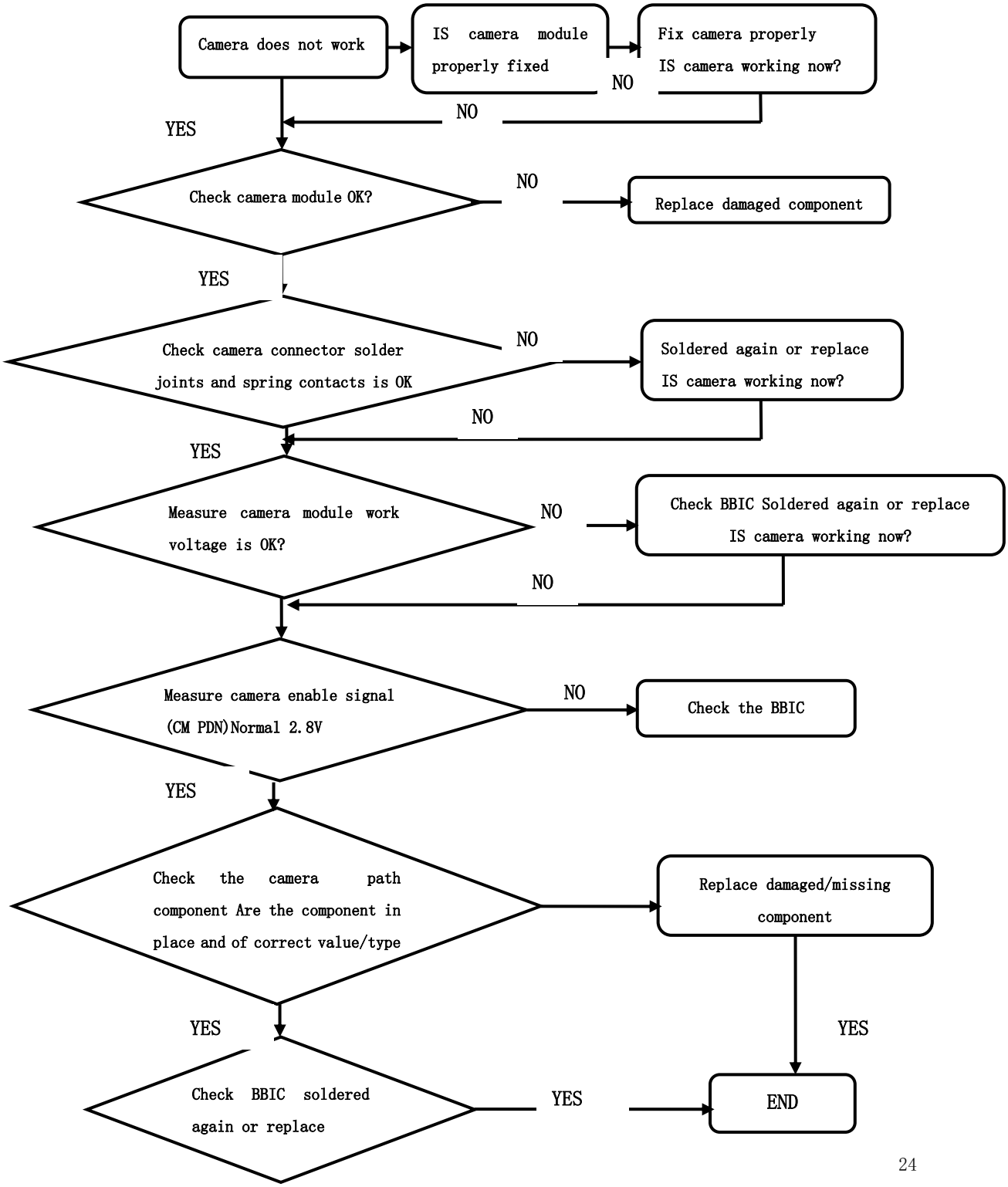




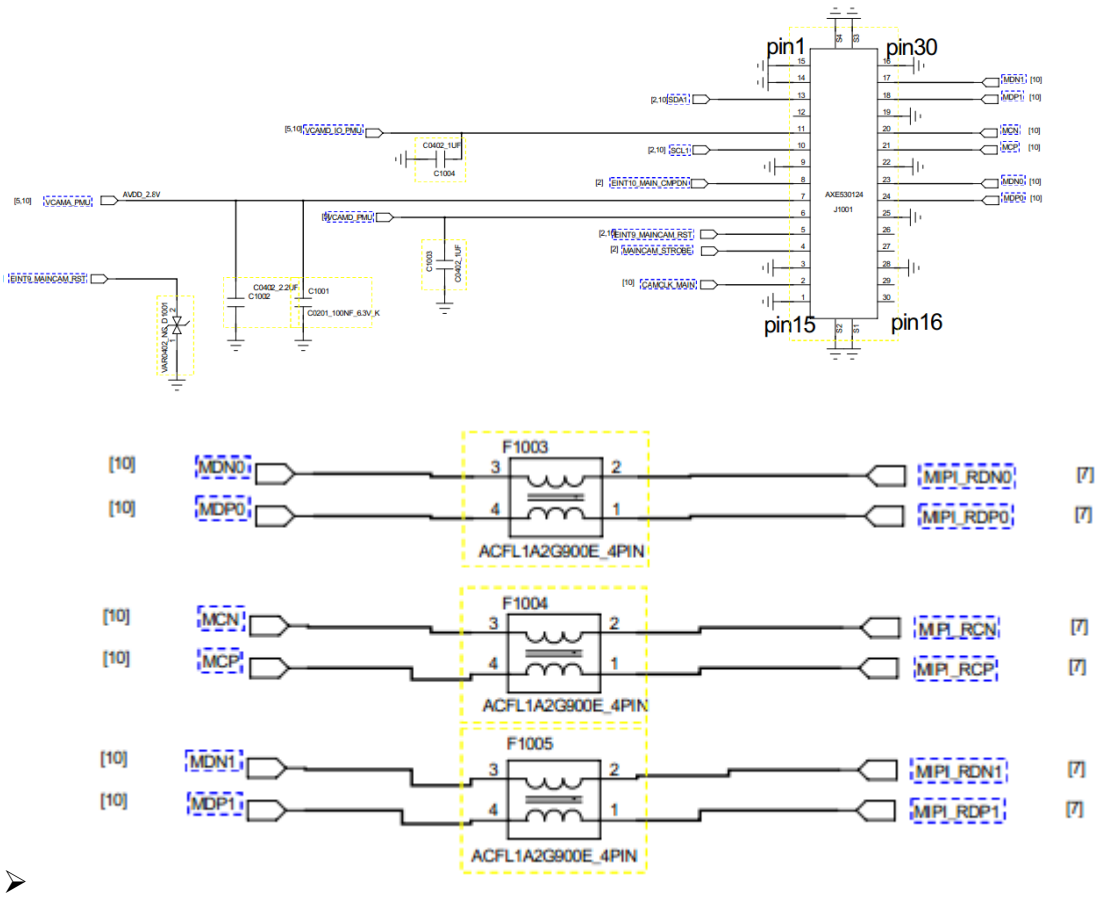
3-1-8. Camera troubleshooting

Troubleshooting flow chart

Main related component: BBIC(U108) , NOR+UTRAM (U401) , CAMERA MODULE.

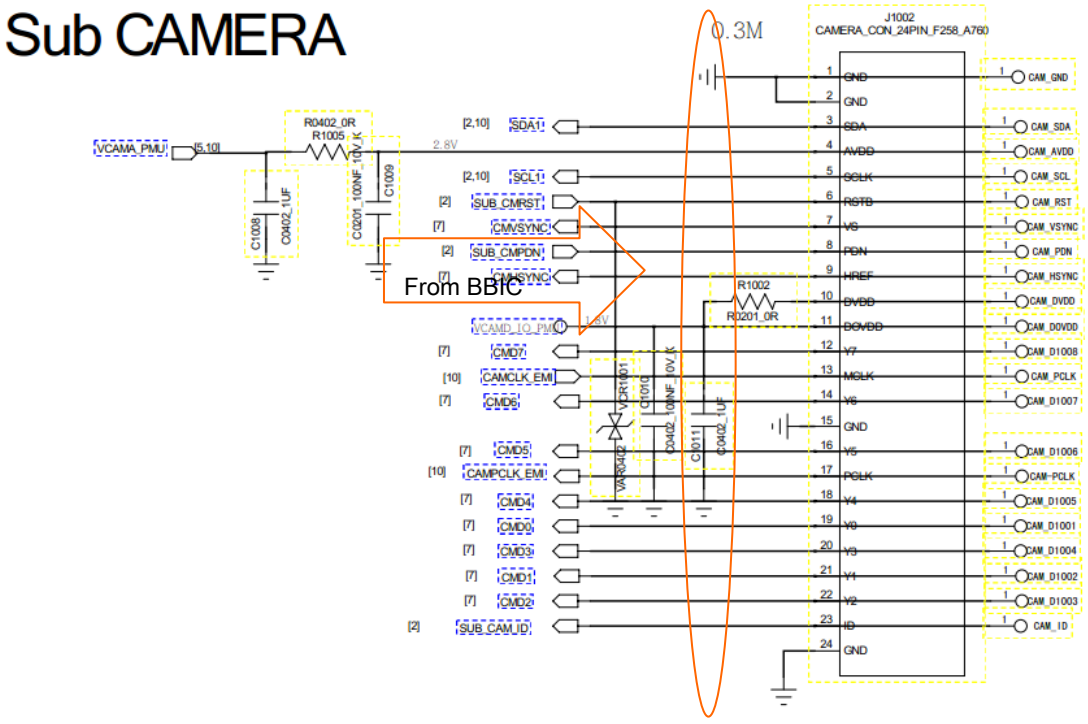


Camera circuit



➢

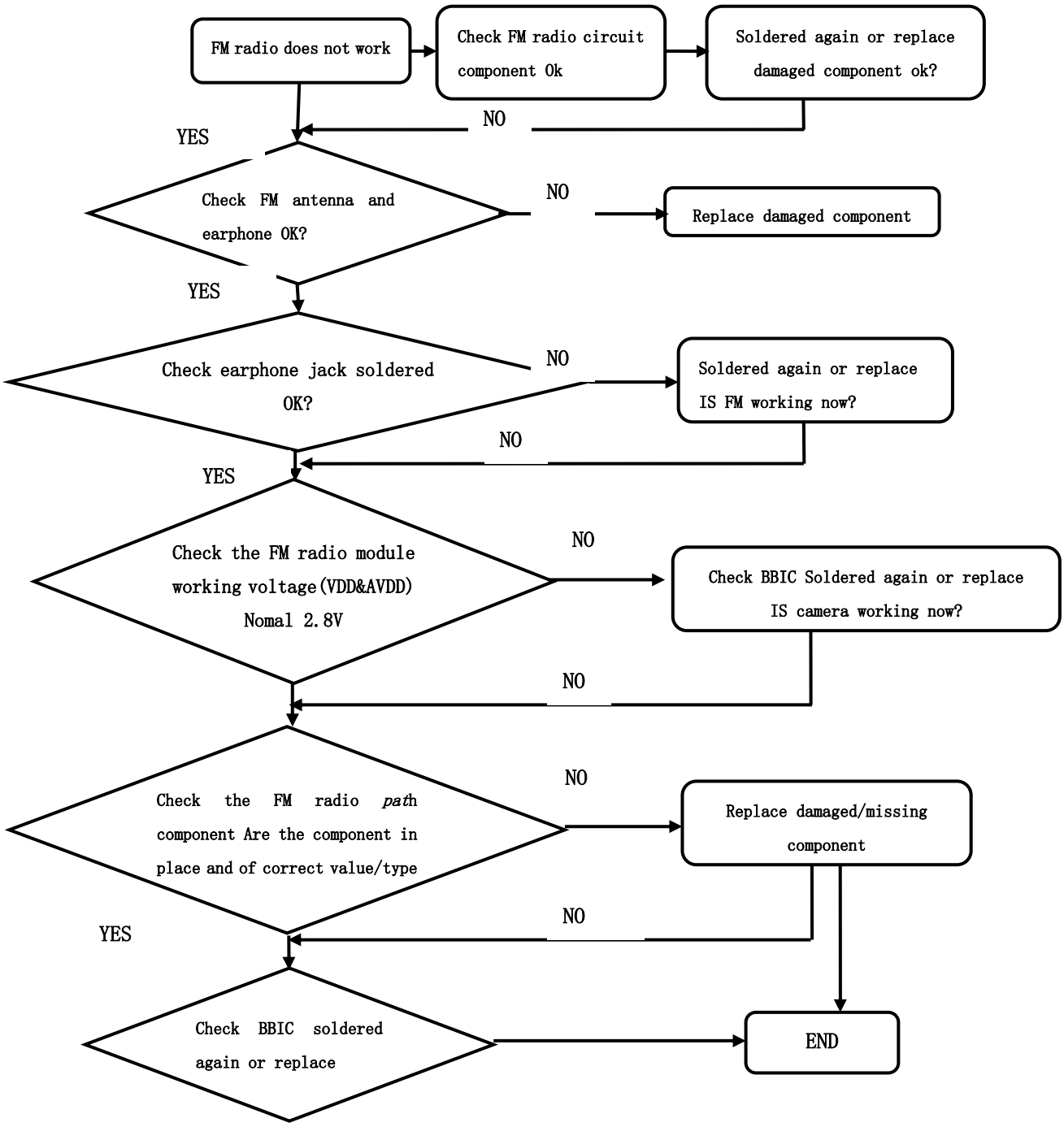
Front Camera circuit



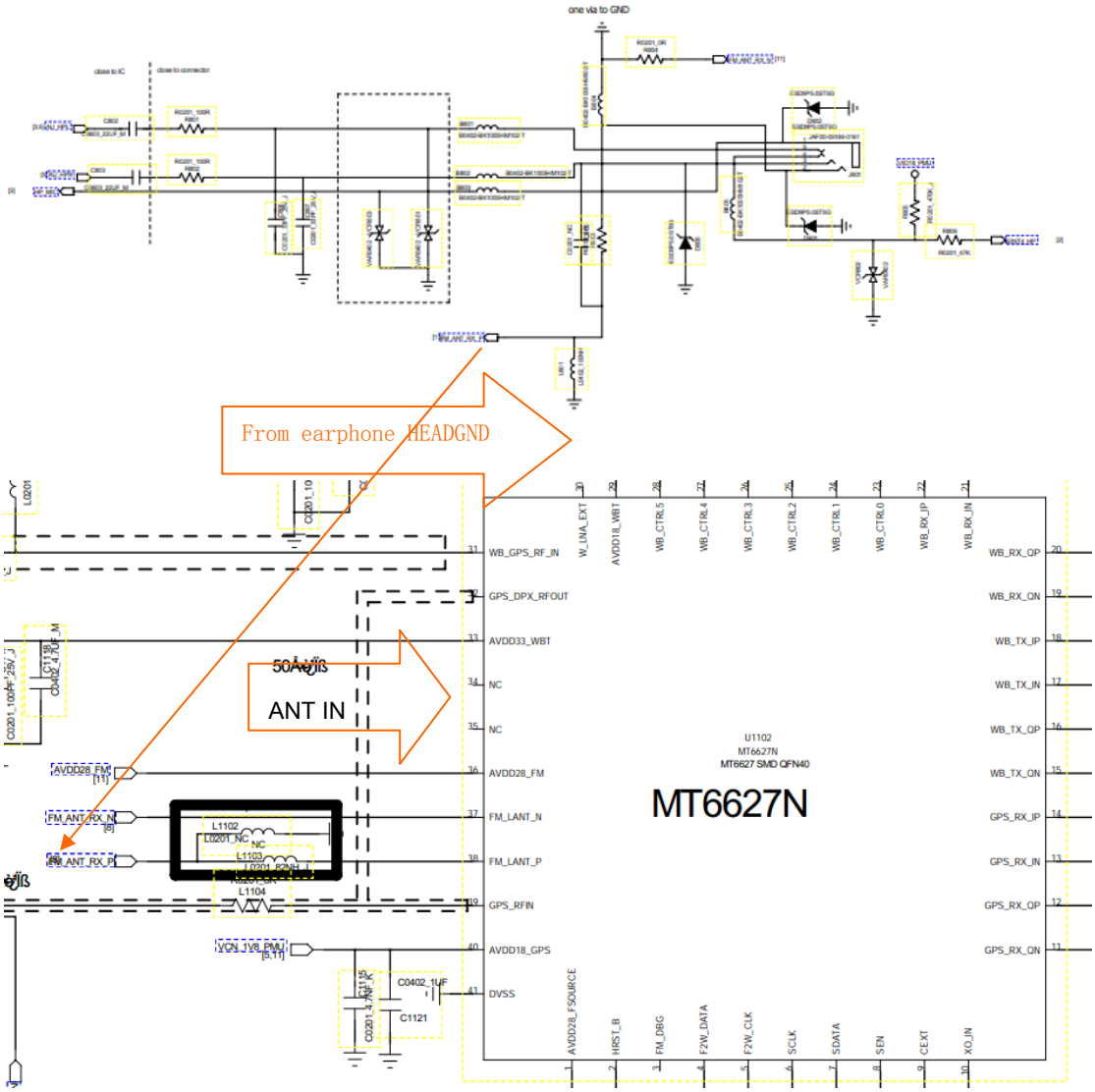
3-1-9. FM radio troubleshooting

Troubleshooting flow chart

Main related component: BBIC(U108)，earphone jack(J801),FM radio(J1102)



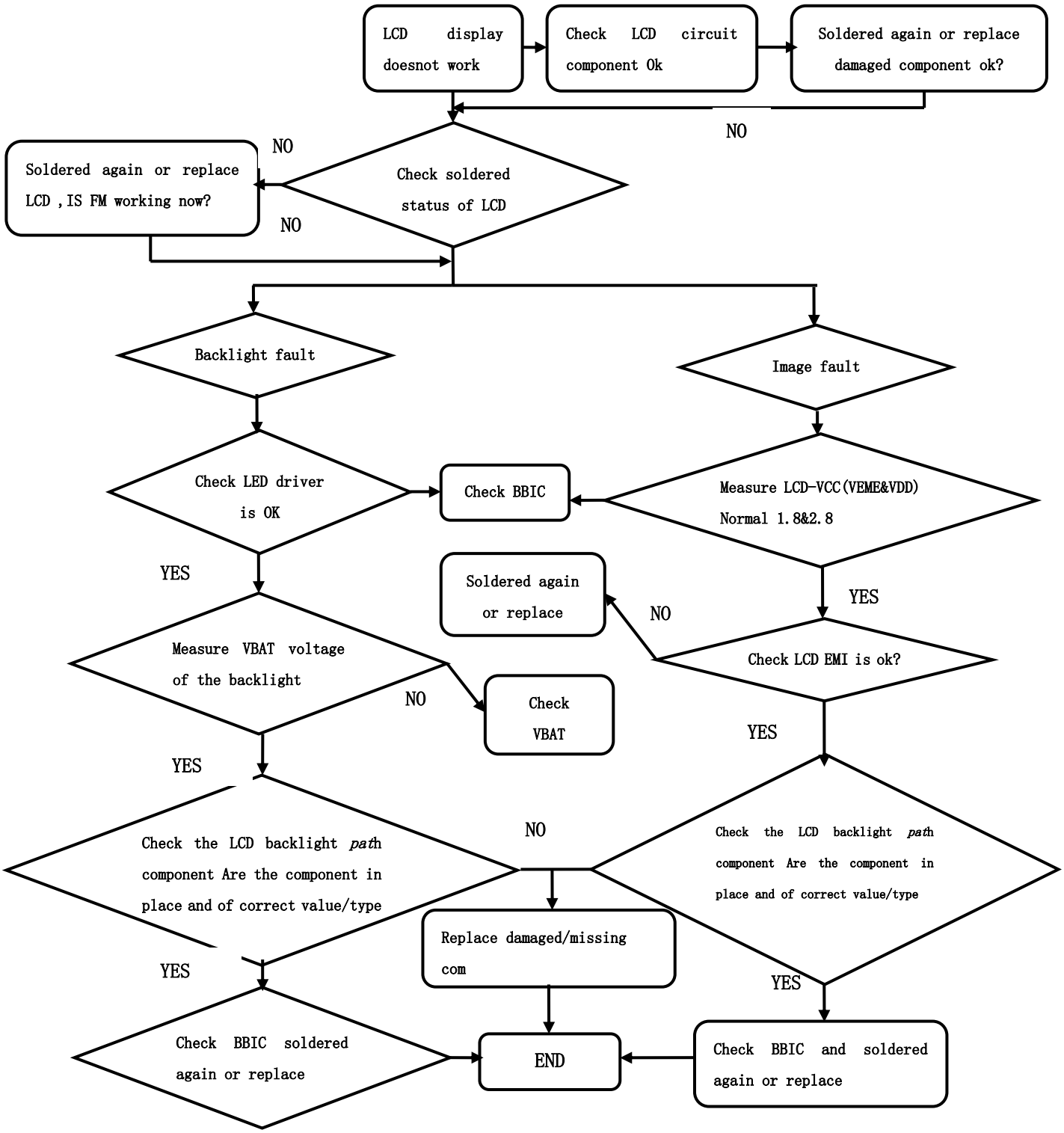
FM Circuit



3-1-10. Display troubleshooting

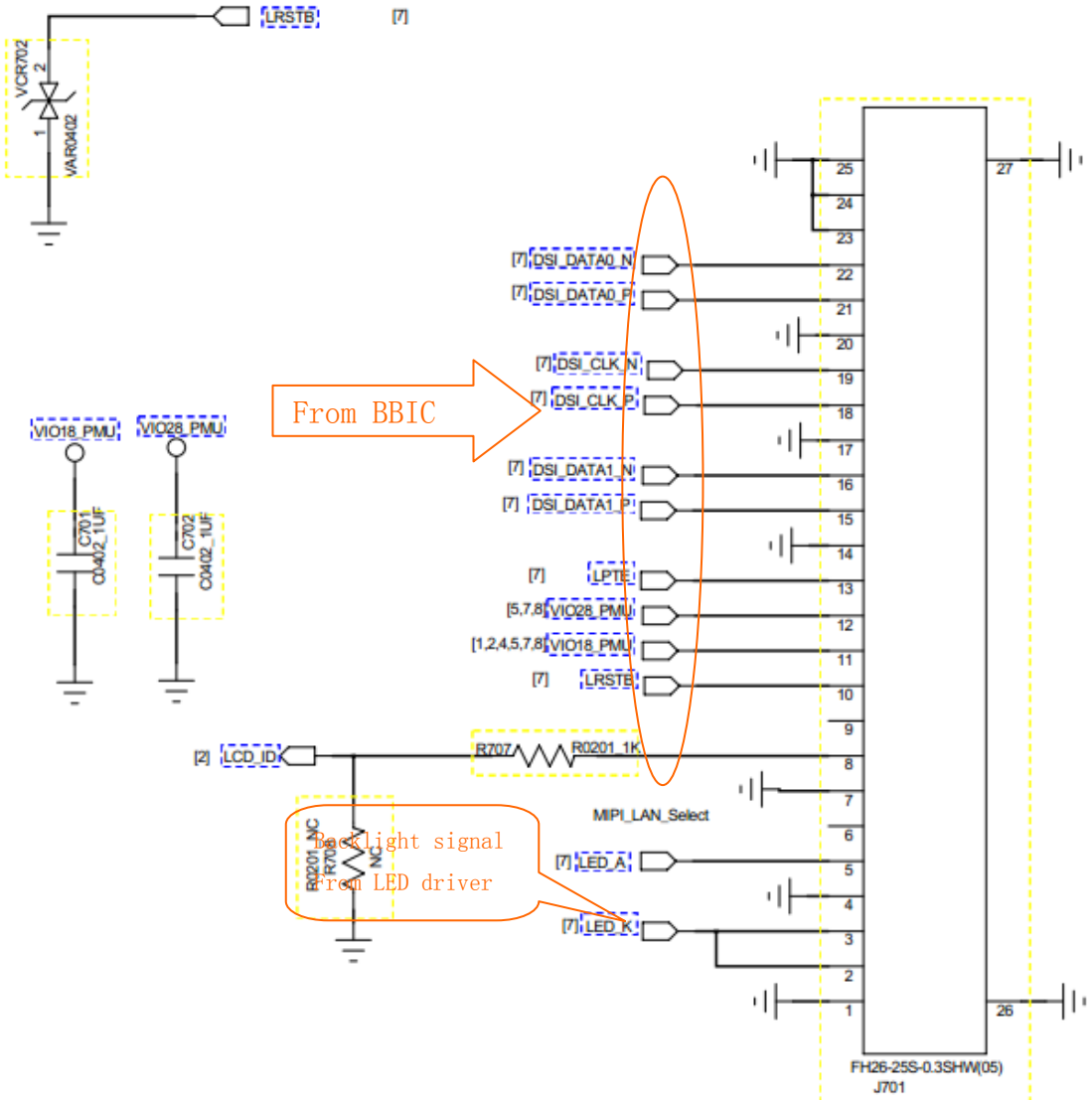
Troubleshooting flow chart

Main related component: BBIC(U108),EMI(F701-F702),LCD.

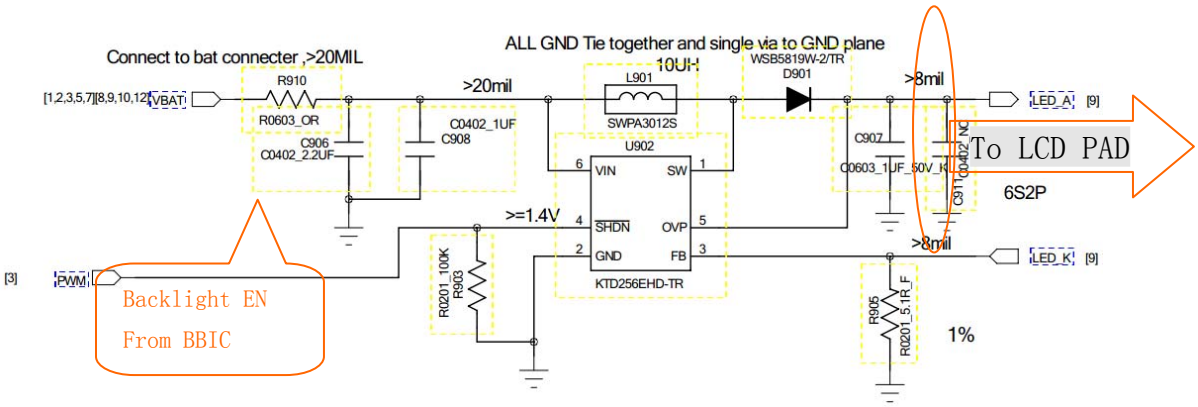


Display Circuit

- LCD Connector circuit



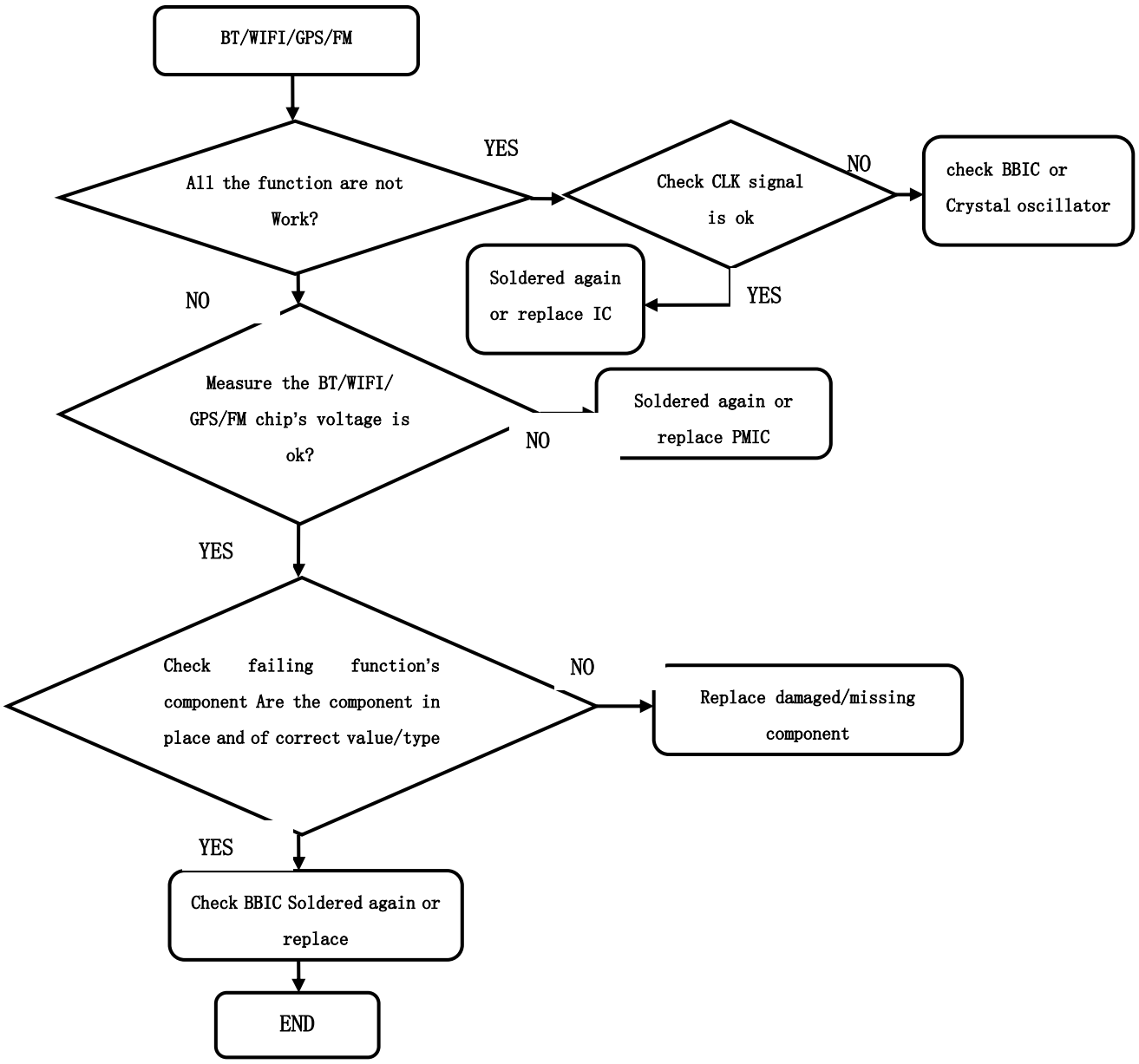
- LCD backlight circuit



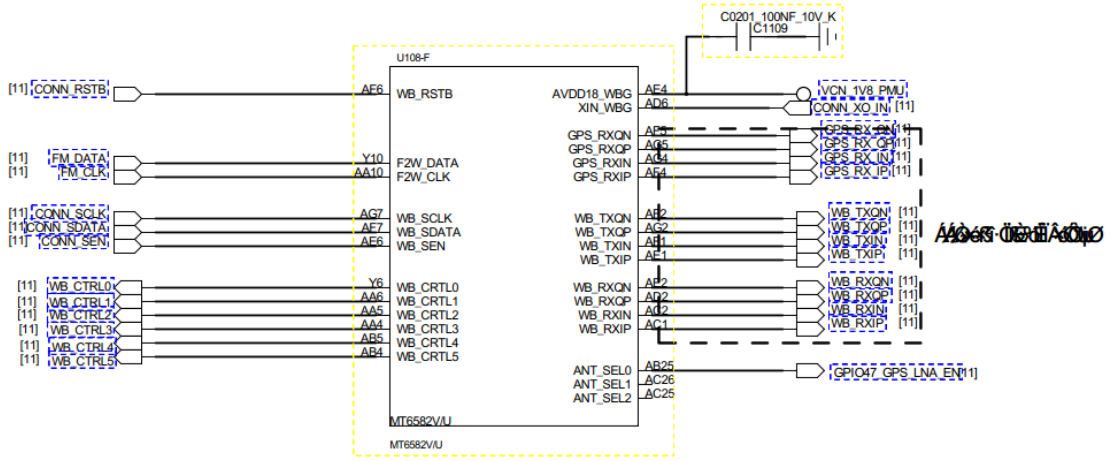
3-1-11. Bluetooth WIFI GPS troubleshooting

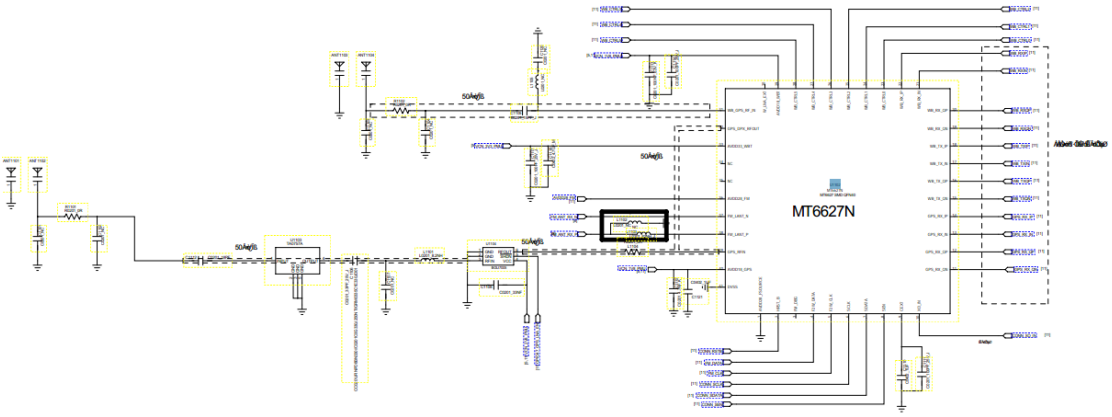
Troubleshooting flow chart

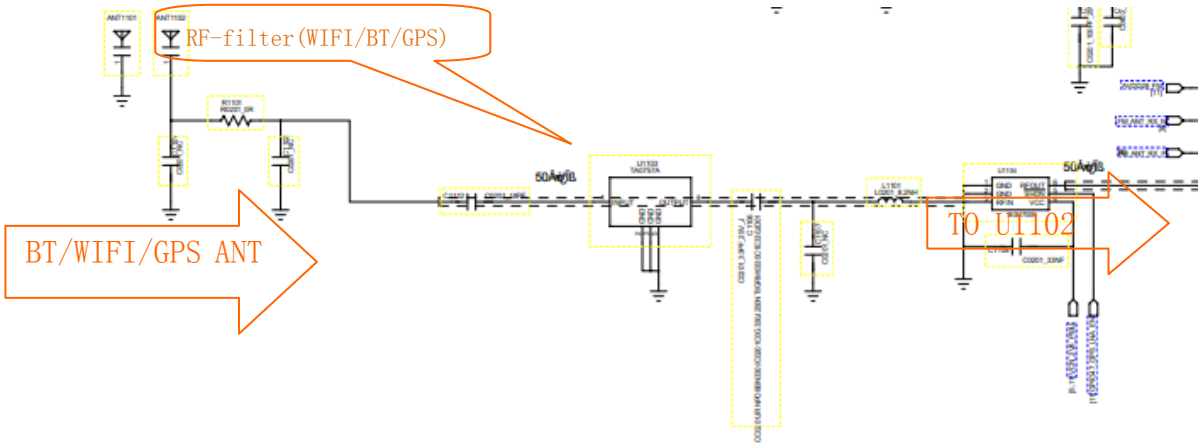
Main related component: BBIC(U108) ,BT/WIFI/GPS MODEM (J1102) , The Clock signal provided by the CPU;



Bluetooth WIFI GPS circuit

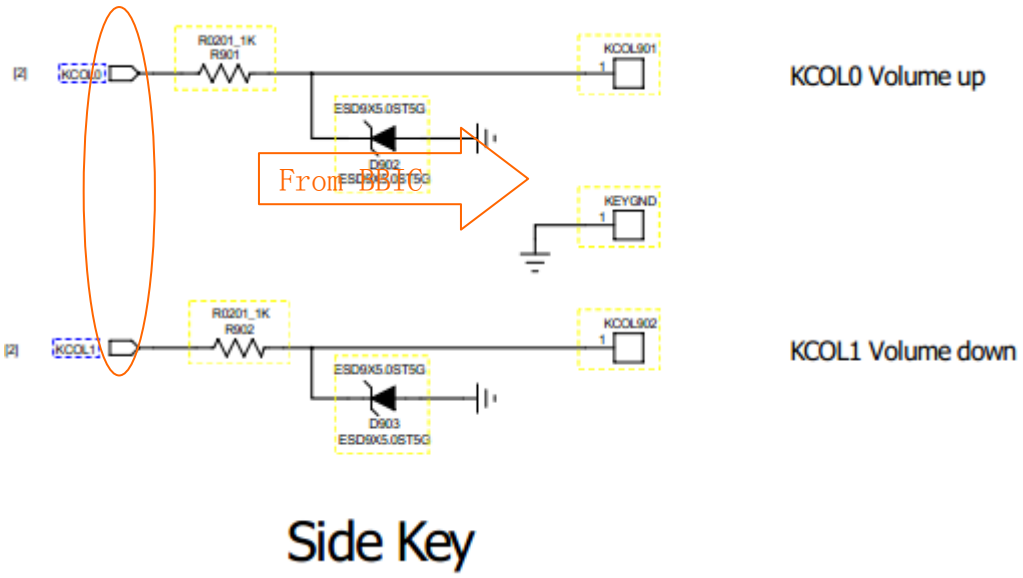






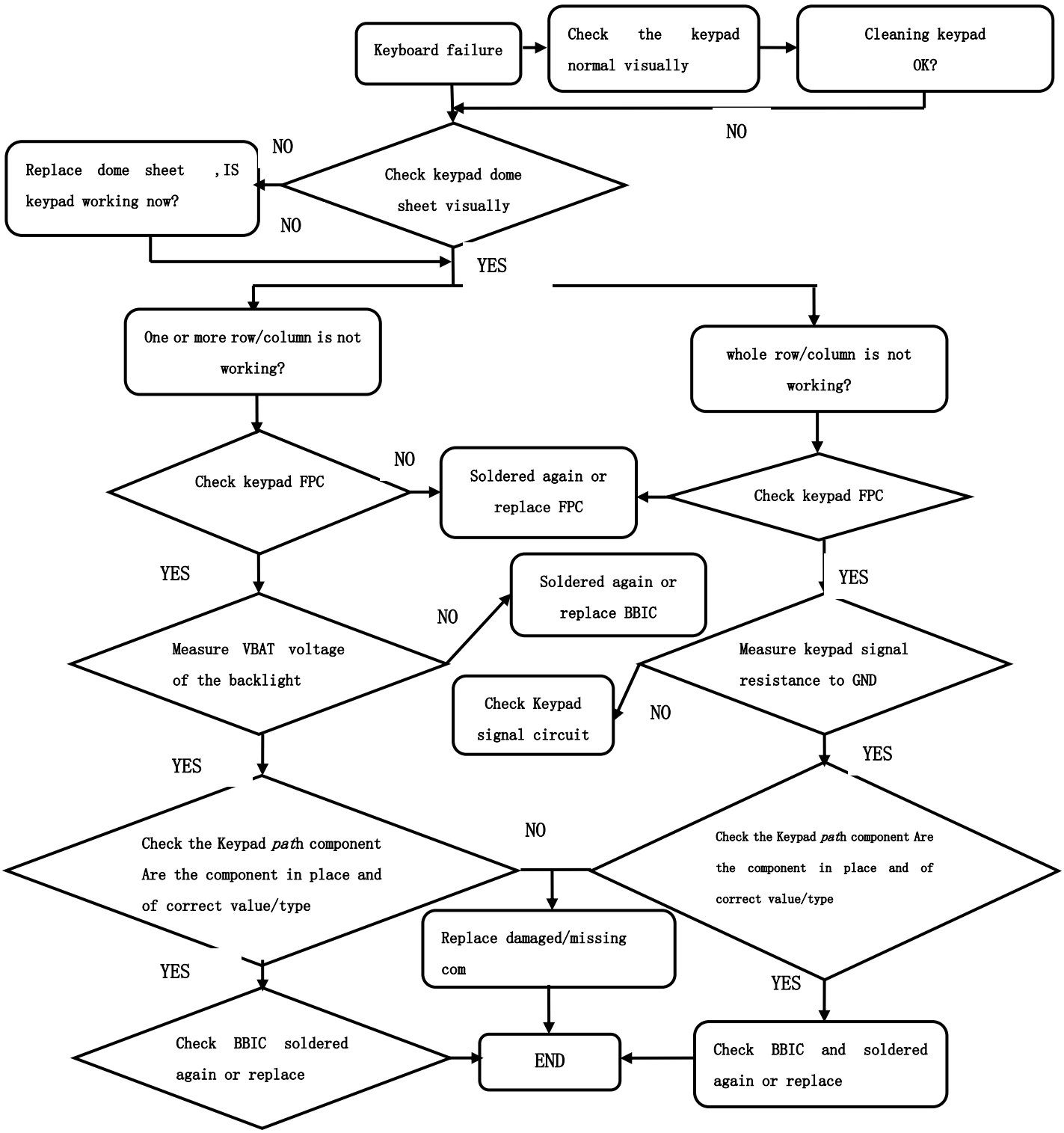
3-1-12. Side health Troubleshooting

Keyboard circuit



Troubleshooting flow chart

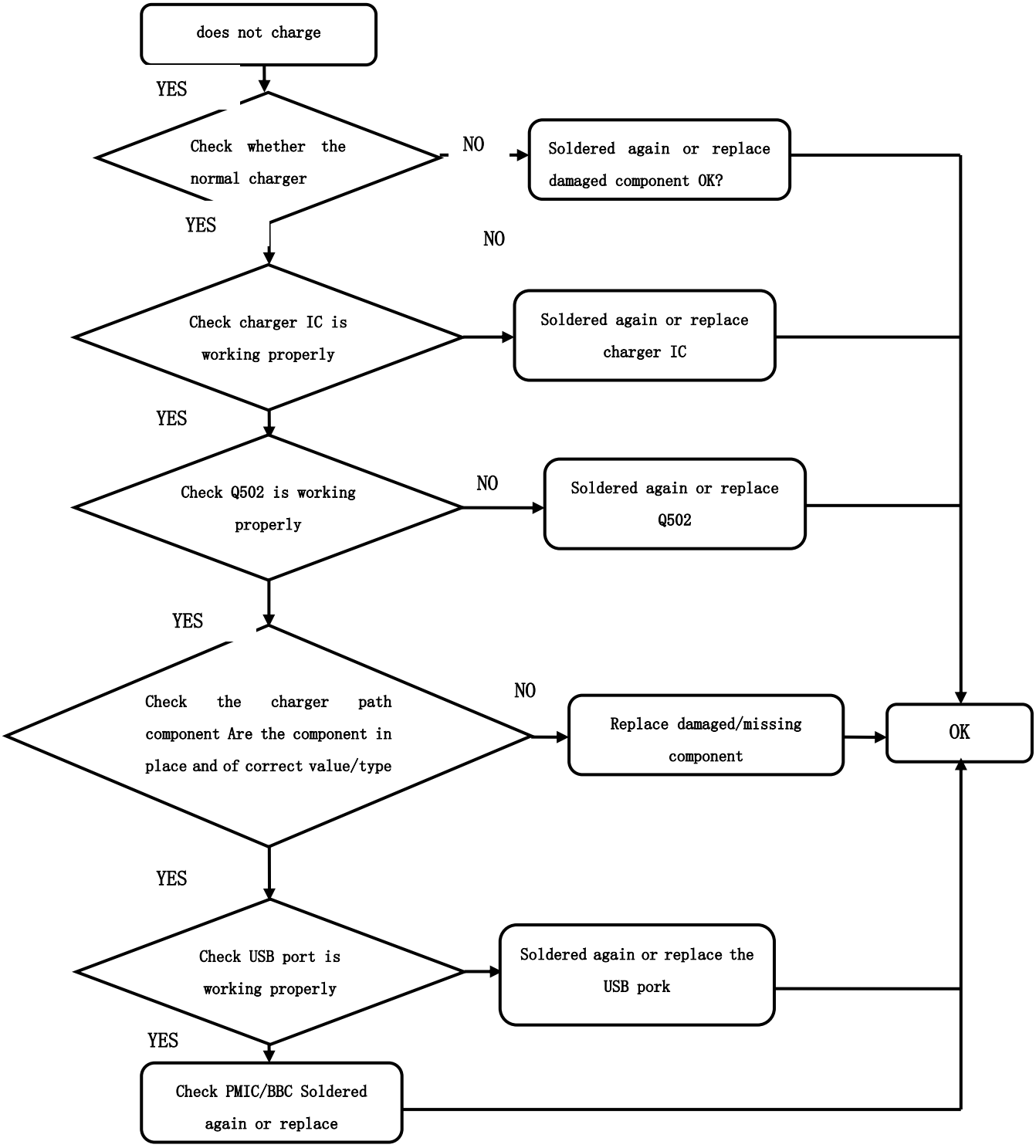
Main related component: BBIC(U108) and keypad FPC



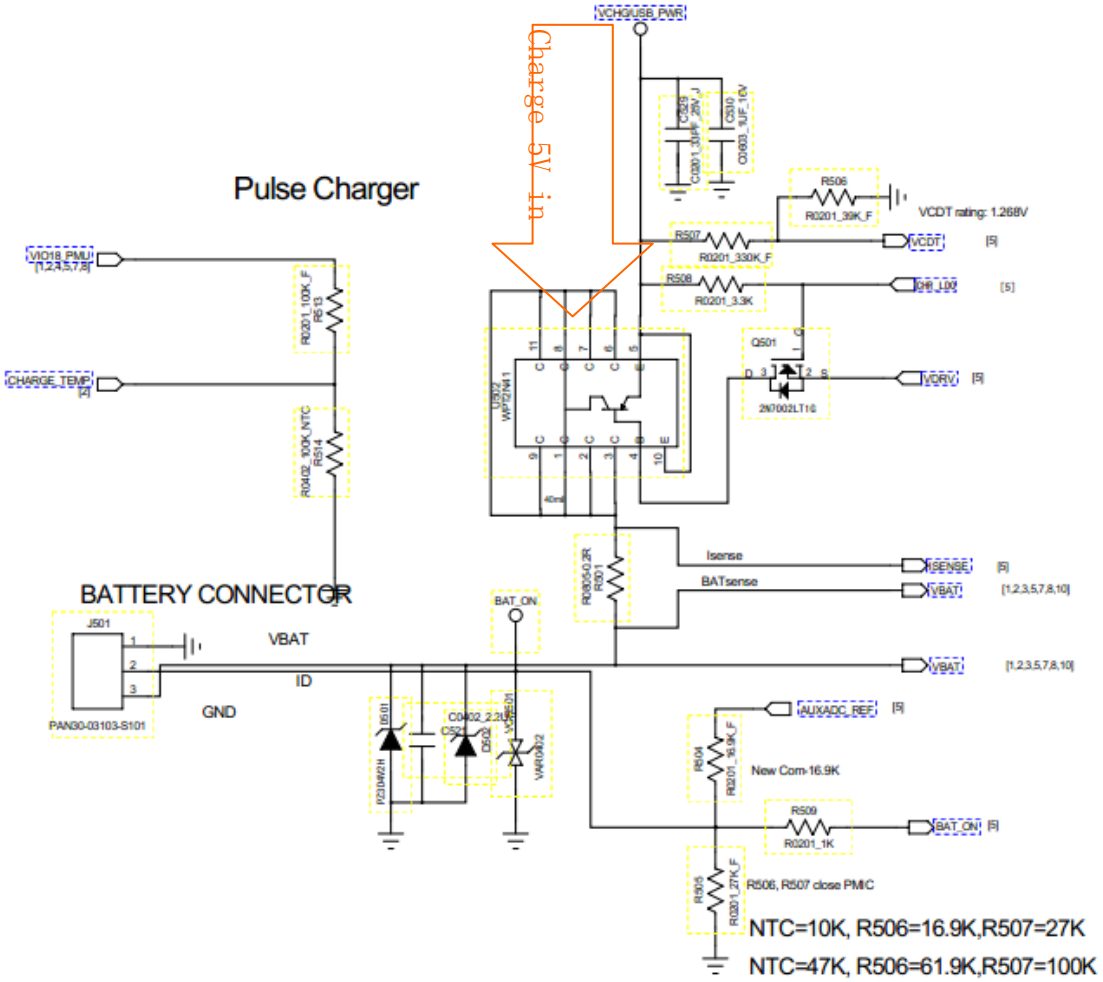
3-1-13. Charge troubleshooting

Troubleshooting flow chart

Main related component: BBIC(U108), USB(J802) , MOSFET (U502) .



Battery charge circuit

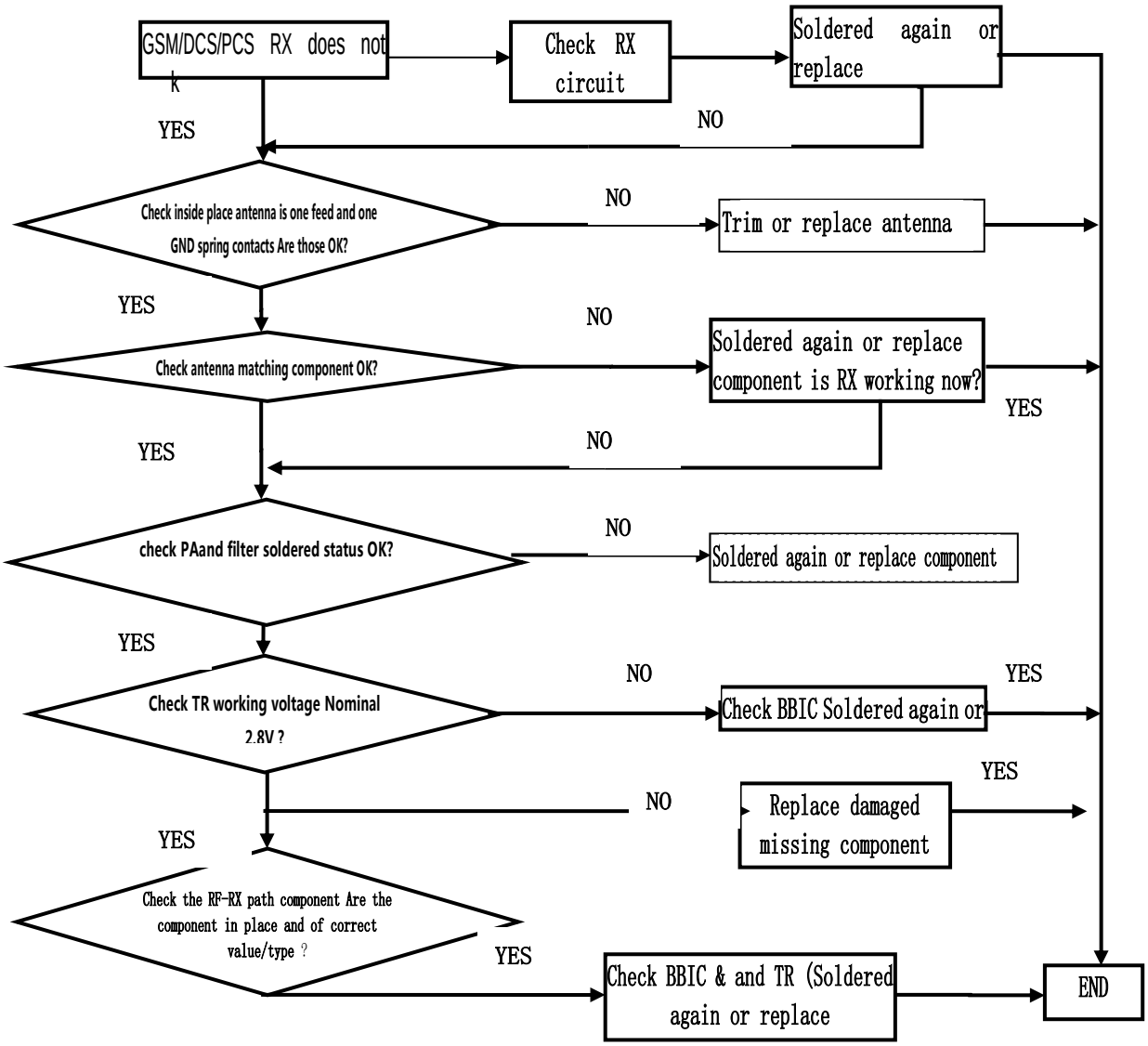


3.2 RF

3-2-1.GSM/DCS RX troubleshooting

Troubleshooting flow chart

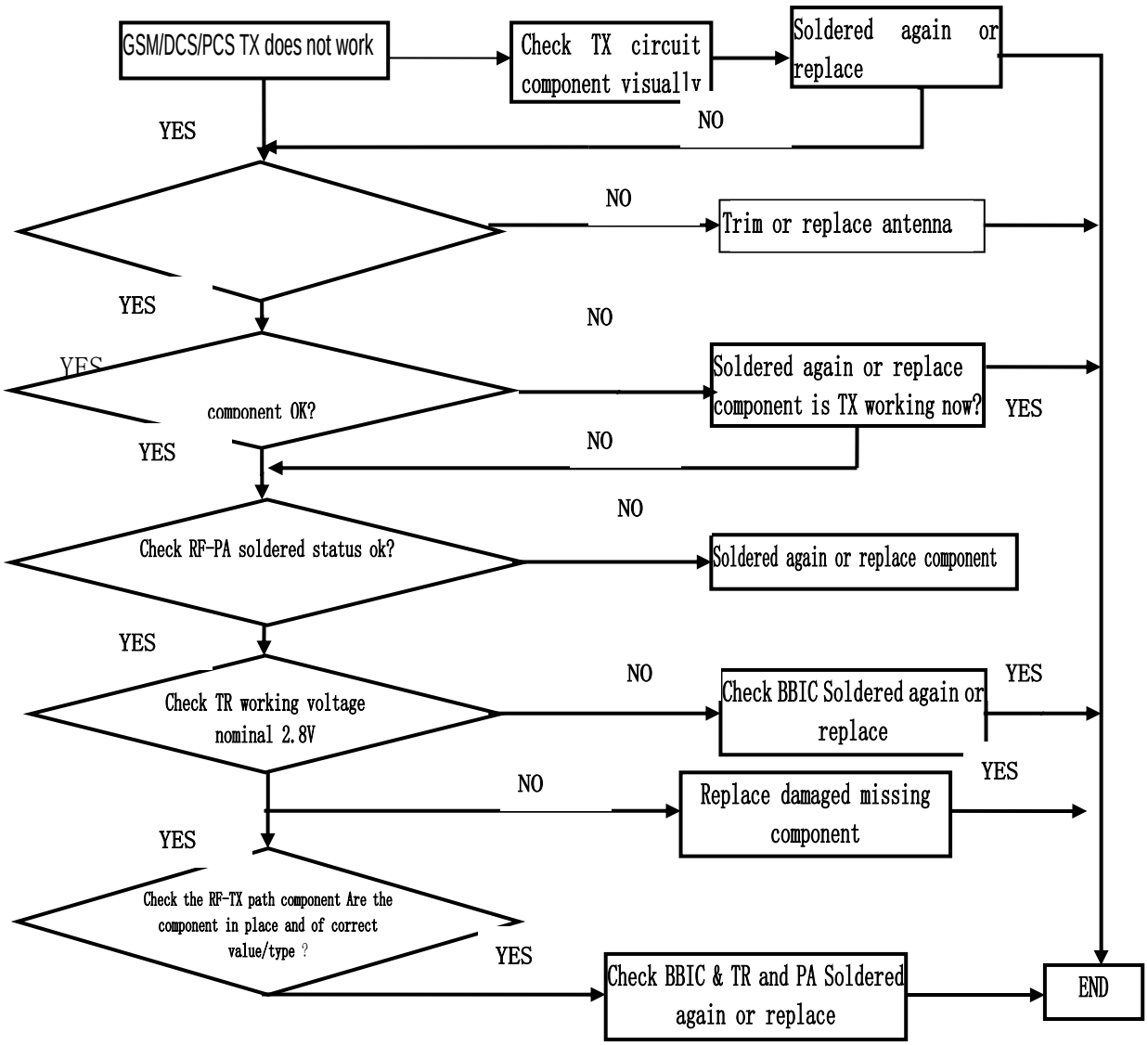
Main related component: BBIC(U108) XTAL CRYSTAL (X101),RF-TR(U201),RF-PA (U101) , RX FILTER (U103)



3-2-2.GSM/DCS TX Part

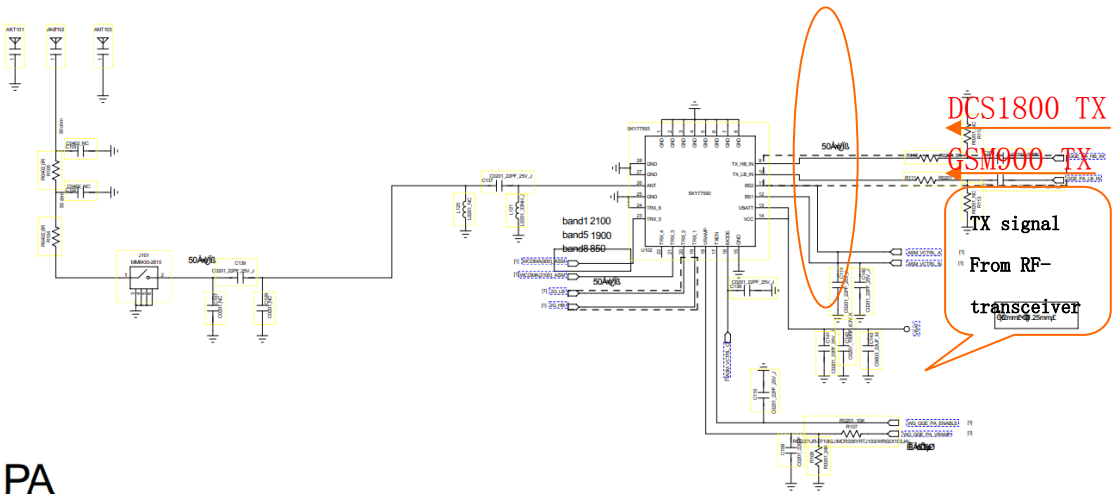
Troubleshooting flow chart

Main related component: BBIC(U108) , XTAL CRYSTAL (X101),RF-TR(U106),RF-PA (U102)



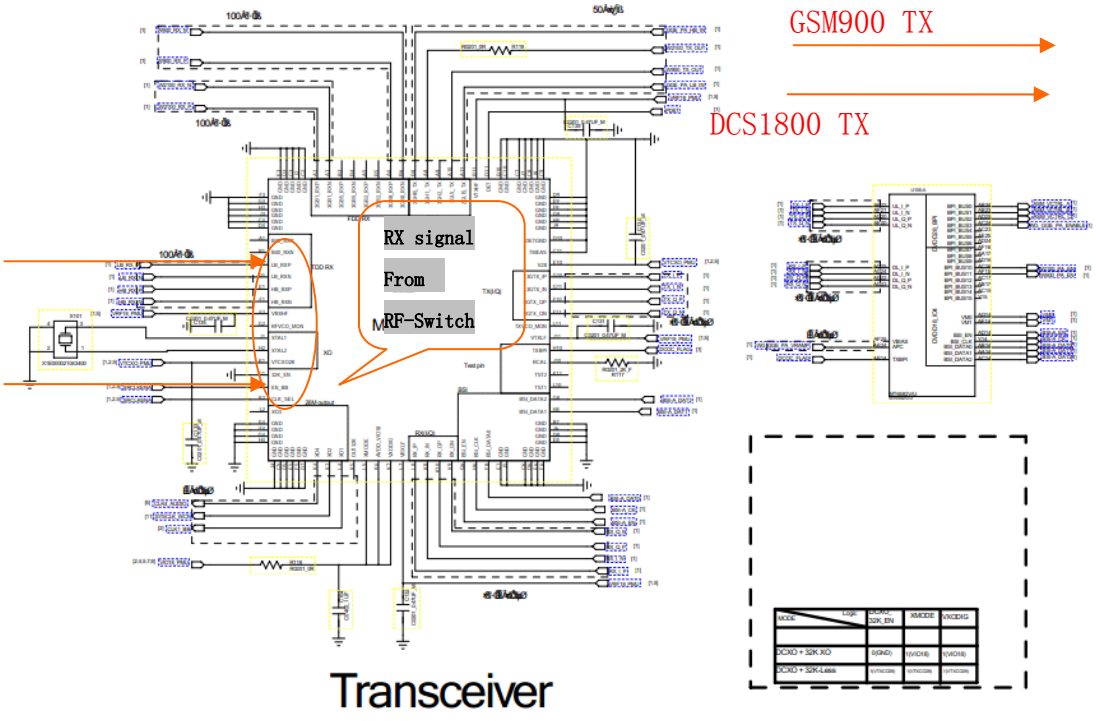
RF Circuit

- RF-PA circuit



PA

- transceiver circuit



Transceiver

4. Main Element Specifications

4-1 Baseband part

4-1-1.BBIC(U108)

System Overview

MT6582 is a highly integrated baseband platform incorporating modem, application processing and connectivity subsystems to enable 3G smart phone applications. The chip integrates a Quad-core ARM® Cortex-A7 MPCore™ operating up to 1.2GHz, an ARM® Cortex-R4 MCU and a powerful multi-standard video accelerator. The MT6582 interfaces to NAND flash memory, LPDDR2 and LPDDR3 for optimal performance and also supports booting from SLC NAND or eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces are included to interface to cameras, touch-screen displays, and MMC/SD cards.

The application processor, a Quad-core ARM® Cortex-A7 MPCore™ which includes a NEON multimedia processing engine, offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Audio supports include FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting Category 14 (21 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates as well as Class 12 GPRS, EDGE.

MT6582 includes four wireless connectivity functions, WLAN, Bluetooth, GPS, and FM receiver. The RF parts of those four blocks are put in the MT6627 chip. With four advanced radio technologies integrated into one single chip, MT6582/MT6627 provides the best and most convenient connectivity solution among the industry. MT6582/MT6627 implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It also supports single antenna sharing among 2.4 GHz antenna for Bluetooth, WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data, and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Platform Features

- **General**
  - Smartphone two MCU subsystems architecture
  - SLC NAND flash and eMMC bootloader
- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A7 MPCore™ operating at 1.2 GHz
  - NEON multimedia processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 1.05V to 1.26V
- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with maximum 491.5 MHz operation frequency
  - 32KB I-cache, 16KB D-cache
  - 256KB TCM (tightly-coupled memory)
  - DSP for running modem/voice tasks, with maximum 240MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control
- **CONN MCU subsystem**
  - Andes N9 processor with 32KB I-cache, 16KB D-cache
- **MD external interfaces**
  - Dual SIM/USIM interface supported
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, …)
- **External memory interface**
  - Supports LPDDR2/3 up to 2GB
  - 32-bit data bus width
  - Memory clock up to 533 MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
- **Security**
  - ARM® TrustZone® Security
- **Connectivity**
  - USB2.0 high-speed dual mode supporting 8 Tx and 8 Rx endpoints
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - 4 UARTs for external devices and debugging interfaces
  - SPI for external devices
  - 3 I2C to control peripheral devices, e.g. CMOS image sensor, or LCM module
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controller supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols
- **Operating conditions**
  - Core voltage: 1.15V
  - Processor DVFS+SRAM voltage : 1.05V~1.26V (Typ. 1.15V ; sleep mode 0.85V)

- I/O voltage: 1.8V/2.8V/3.3V
- Memory: 1.2V
- NAND: 1.8V/2.8V
- LCM interface: 1.8V
- Clock source: 26-MHz, 32.768-kHz

- **Package**
  - Type: FCCSP
  - 10.6mm x 11mm
  - Height: 1.0mm maximum
  - Ball count: 475 balls
  - Ball pitch: 0.4mm

1.2 MODEM Features

- **3G UMTS FDD supported features (with MT6166)**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - Two DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 6, throughput up to 5.7Mbps
  - Downlink Cat. 14, throughput up to 21Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength (shared by 2G & 3G modem)
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced sidetone oscillation reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (single antenna interference cancellation) technology
  - Supports VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

1.3 Multimedia Features

- **Display**

- Supports landscape or portrait panel resolution up to qHD (960x540)
- MIPI DSI interface (4 data lanes)
- Embedded LCD gamma correction
- Supports true colors
- 4 overlay layers with per-pixel alpha channel and gamma table
- Supports spatial and temporal dithering
- Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
- Supports color enhancement
- Supports adaptive contrast enhancement
- Supports image/video/graphic sharpness enhancement
- Supports dynamic backlight scaling

- **Graphics**
  - OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 53.25M tri/sec and 1000M pixel/sec @ 500MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Integrated image signal processor supports 8 MP
  - Supports electronic image stabilization
  - Supports video stabilization
  - Supports preference color adjustment
  - Supports noise reduction
  - Supports lens shading correction
  - Supports auto sensor defect pixel correction
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Sampling rates supported: 8kHz to 48kHz
  - Supports AE/AWB/AF
  - Supports edge enhancement (sharpness)
  - Supports face detection and visual tracking
  - Supports zero shutter delay image capture
  - Supports capturing full size image when recording video (up to 8M sensor)
  - Supports MIPI CSI-2 high-speed camera serial interface with 4 data lane (for main) + 2 data lane (for sub)
  - Hardware JPEG encoder: Baseline encoding with 120M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p@30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX3/DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - VP8 decoder: 1080p @ 30fps/40Mbps
  - VC-1 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps (SW)
  - H.263 encoder: D1 @ 30fps (SW)

  - Sample formats supported: 8-bit/16-bit, Mono/Stereo
  - Interfaces supported: DAI, I2S, PCM
  - 4-band IIR compensation filter to enhance loudspeaker responses

- Proprietary audio post-processing technologies: BesLoudness, Android built-in post processing
- Audio encode: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decode: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC input
  - Digital MIC input

1.4 BT/WLAN/GPS/FM with MT6627 Features

- **Common**
  - Self calibration
  - Single TCXO and TSX for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - OS supported: Android
  - Intelligent BT/WLAN coexistence scheme
  - Single antenna support for WLAN/Bluetooth/GPS

- **WLAN**
  - Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w Protected Managed Frames
  - Supports WiFi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated PA with max 21dBm output power
  - Typical -77.5 dBm 2.4GHz receiver sensitivity at 11g 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 10dBm (class 1) transmit power and Balun
  - Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet loss concealment (PLC) function for better voice quality

- Low-power scan function to reduce the power consumption in scan modes

- **GPS**
  - Supports GPS/QZSS/SBAS (WAAS/MSAS/EGNOS/GAGAN)
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 8 in-band tones
  - Supports TCXO
  - Supports co-clock with AP/MD
  - 5Hz update rate

- **FM**
  - 76-108MHz with 50kHz step
  - Supports RDS/RBDS
  - Digital stereo modulator/demodulator
  - Simplified digital audio interface (I2S)
  - Fast seek time 30ms/channel
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf ((S+N)/N=26dB)
  - Audio S/N 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer.
  - Fully integrated in one IPD die
  - Supports single and dual antenna operation.

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter.
  - Fully integrated in one IPD die
  - Supports single and dual antenna operation.

1.5 General Descriptions

MediaTek MT6582 is a highly integrated 3G System-on-chip (SoC) which incorporates advanced features e.g. HSPA R8 modem, Quad-core ARM® Cortex-A7 MPCore™ operating at 1.2 GHz, 3D graphics (OpenGL|ES 2.0), 8M camera ISP, LPDDR2/3 533 MHz and high-definition 1080p video decoder. MT6582 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

World-leading technology

Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6582 is the brand-new generation smart phone SoC integrating MediaTek HSPA R8 modem, 1.2GHz Quad-core ARM® Cortex-A7 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in features, high-valued product

To enrich the camera features, MT6582 equips a 8M camera ISP with advanced features e.g. auto focus, anti-handshake, auto sensor defect pixel correction, continuous video AF, face detection, burst shot, optical zoom, panorama view and 3D photos.

Incredible browser experience

The 1.2 GHz Quad-core ARM® Cortex-A7 MPCore™ with NEON multimedia processing engine brings PC-like browser experiences and helps accelerate OpenGL|ES 2.0 3D Adobe Flash 10 rendering performance to an unbeatable level.

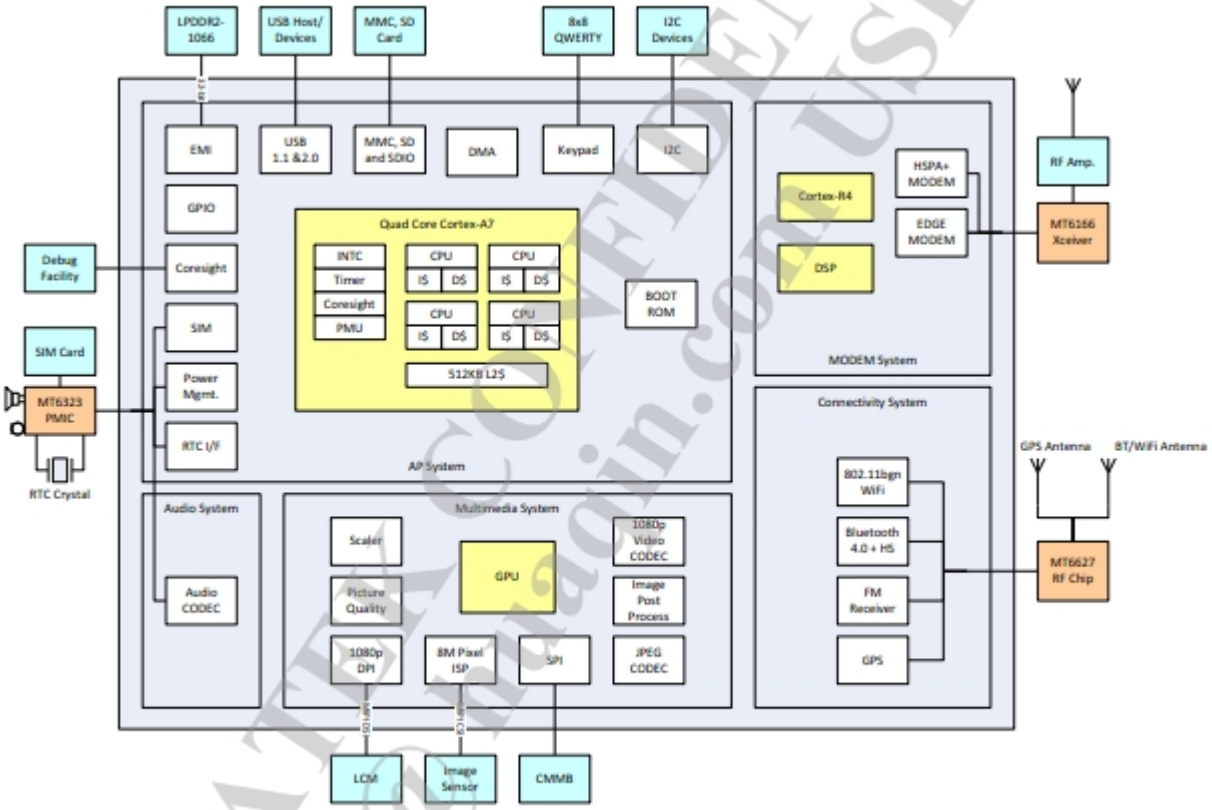
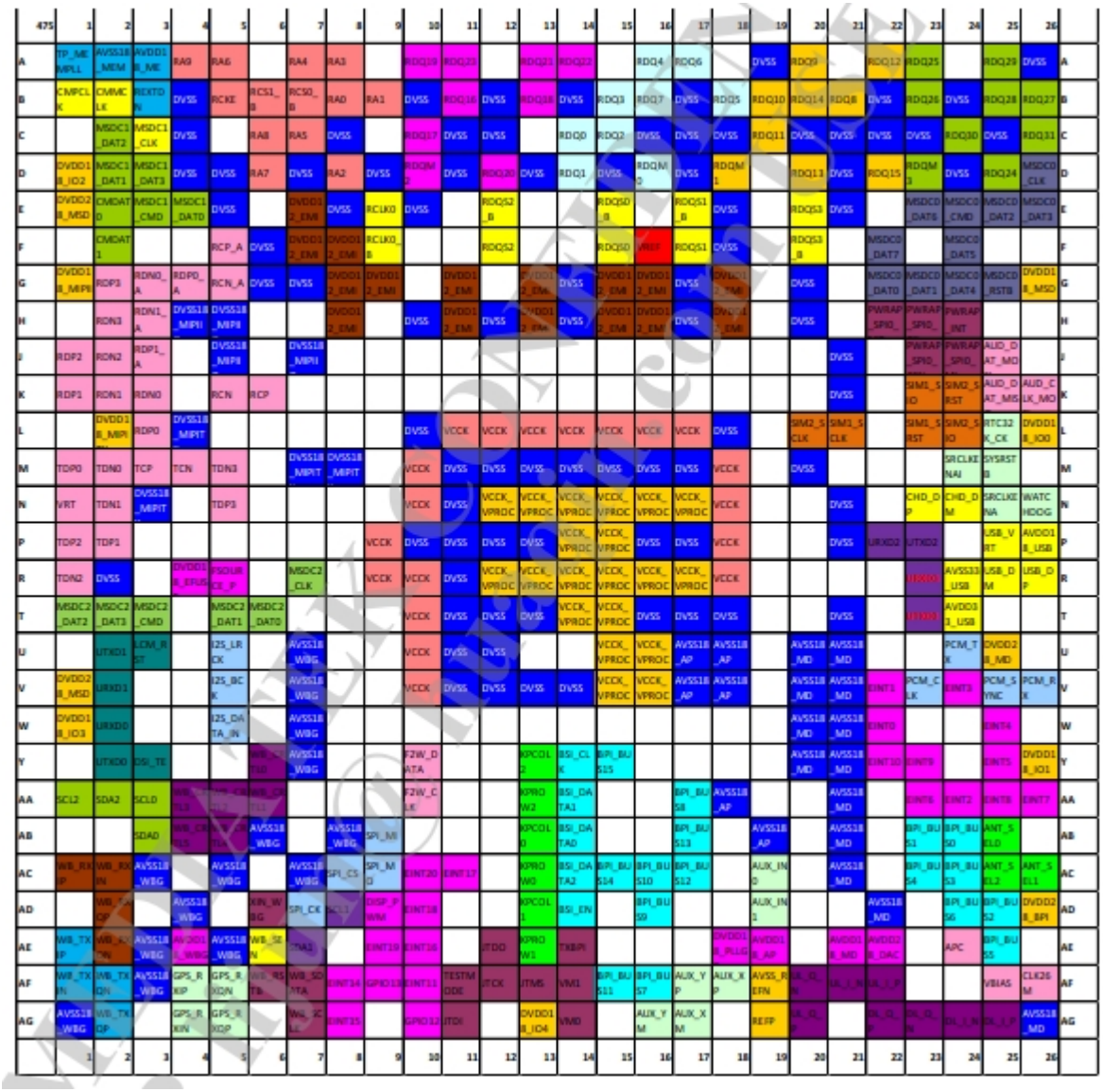


Figure 1-1: Block diagram of MT6582

Pin Outs



4-1-2 Power Management Control(U501)

1.1 Features

- Handles all 2G/3G/smart phone baseband power management
- Input range: 3.4 ~ 4.5V
- 3 buck converters and 23 LDOs optimized for specific 2G/3G/smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC and high-power/quality audio amplifier
- 32K RTC crystal oscillator for system timing, 1.8 and 2.8V clock buffer output
- Multiple function GPIO
- Flexibility for various configurations of indicator LED current source: 4ISINK
- SPI interface
- Li-ion battery charging function
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog timer
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- VFBGA - 145L package

1.2 Applications

Ideal for power management of 2G, 3G, smart phones and other portable systems.

1.3 General Descriptions

MT6323 is a power management system chip optimized for 2G/3G handsets and smart phones, especially based on the MediaTek MT6572 system solution. MT6323 contains 3 buck converters and 23 LDOs, which are optimized for specific 2G/3G/smart phone subsystems.

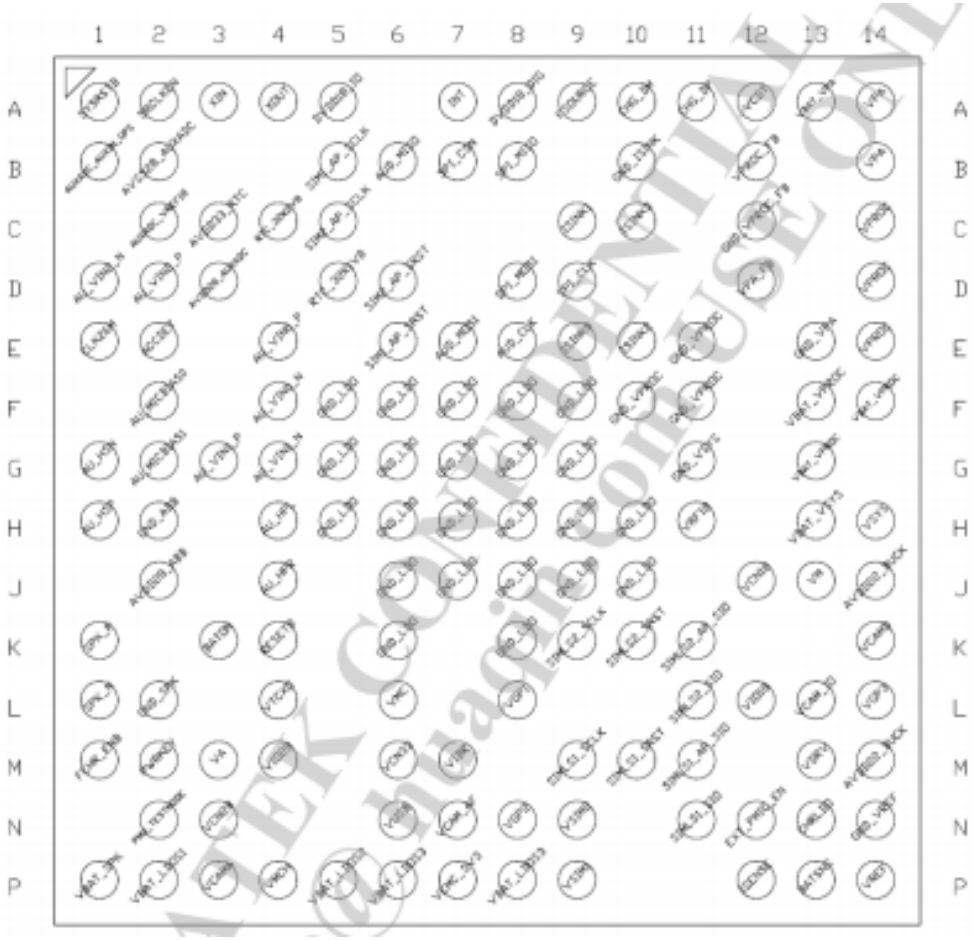
MT6323 provides mono 0.7W into 8Ω, high efficiency Class AB/D audio amplifiers and flexibility for various applications of indicator LED drivers. It supports up to 4 channel LEDs with independent controlled. Flexible control includes: register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6323 is optimized for maximum battery life. It allows the RTC circuit to stay alive without a battery for several hours. The battery charger in MT6323 supports lithium- ion (Li-ion) battery and provides pre-charge indication. The charger input voltage can be up to 10V and allows USB charging, too.

Some multi-purpose pins enable MT6323 to be configured in various applications.

MT6323 adopts SPI interface and SRCLKEN control pin to control buck converters, LDOs, Class AB/D, various drivers and charger. Besides, it provides enhanced safety control and protocol for handshaking with BB.

MT6323 is available in a VFBGA - 145L package. The operating temperature ranges from -25 to +85°C.



4-1-3. MT6627 IC(U1102)

➢ Features

- MT6627 is 4-in-1 connectivity RF chip which contains front-ends of a 2.4GHz WiFi and Bluetooth transceiver, a GPS/Glonass receiver, and an FM receiver.
- MT6627 supports integrated passive device to save footprint on PCB and cost due to WiFi / Bluetooth / GPS external BoM (bill of materials) in a 40-pin QFN package.
- Supports WiFi external LNA and GPS external LNA.

WLAN

- Single-band (2.4GHz) single stream 802.11 b/g/n RF
- Support WiFi and Bluetooth TDD operation and single-antenna topology with integrated TR-switch
- Integrated PA with max 22 dBm CCK output power
- Typical RX sensitivity with companion chip modem: -77.5 dBm at 11g 54Mbps mode
- Support external LNA with an auxiliary RX input
- Integrated power detector to support per packet TX power control
- Built-in calibrations for PVT variation
- One fully integrated frequency synthesizer for both WiFI/BT supporting multiple crystal clock frequencies

Bluetooth

- Bluetooth specification v2.1+EDR
- Bluetooth specification 3.0+HS compliance
- Bluetooth v4.0 Low Energy (LE)
- Integrated PA with 10dBm (class 1) transmit power
- Typical Rx sensitivity with companion chip modem: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
- Low-power scan function to reduce the power consumption in scan modes

FM

- 65-108MHz with 50kHz step
- Supports RDS/RBDS
- Digital stereo modulator/demodulator
- Digital audio interface (I2S)
- Fast seek time 30ms/channel
- Stereo noise reduction
- Audio sensitivity 5dBμVemf ((S+N)/N=26dB)
- Audio S/N 60dB
- Anti-jamming
- Integrated short antenna

GPS

- RF supports GPS, GALILEO, GLONASS & BEIDOU

- Built-in calibrations for PVT variation
- Typical RX tracking sensitivity of -165dBm.
- Support external LNA
- Multi-mode filters for different GNSS receiver modes.

IPD

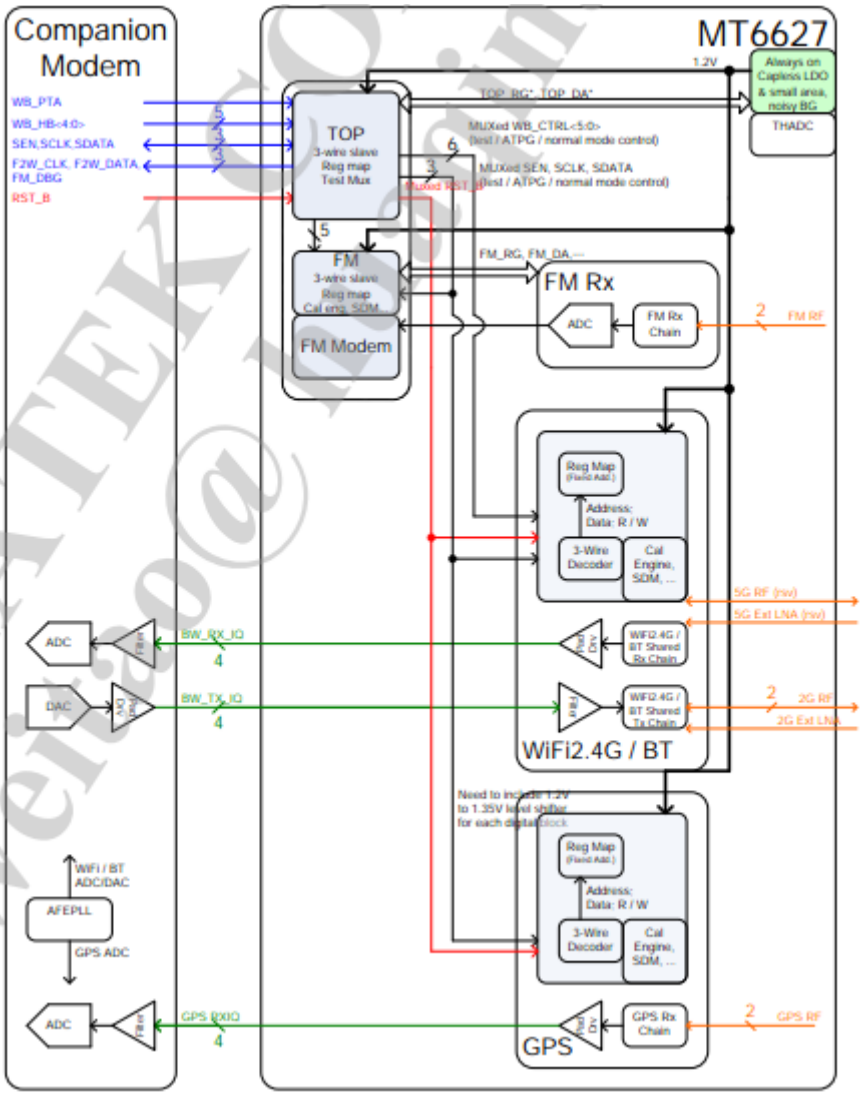
WBT IPD

- Integrated matching network, balance band-pass filter, GPS-WBT diplexer.
- Fully integrated in one IPD die
- Support single and dual antenna operation.

GPS IPD

- Integrated high-pass type matching network and 5th-order ellipse low-pass filter.
- Fully integrated in one IPD die
- Support single and dual antenna operation.

MT6627 Block diagram



4-1-4. Charge IC(U502)

WPT2N41

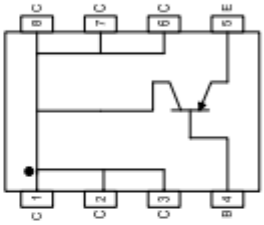
Single, PNP, -30V, -3A, Power Transistor

Http//:www.willsemi.com

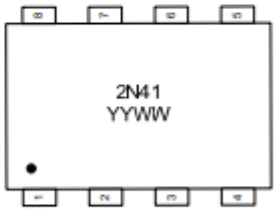
Descriptions

The WPT2N41 is PNP bipolar power transistor with very low saturation voltage. This device is suitable for use in charging circuit and other power management. Standard Product WPT2N41 is Pb-free.

PDFN3x2-8L



Pin configuration (Top view)



2N41 = Device code
YY = Year
WW = Week
Marking

Features

- Ultra low collector-to-emitter saturation voltage
- High DC current gain >100
- 3A continue collector current
- Small package PDFN3x2-8L.

Applications

- Charging circuit
- Power regulator
- Other power management in portable equipments

Order information

Device	Package	Shipping
WPT2N41-8/TR	PDFN3x2-8L	3000/Reel&Tape

0

Absolute maximum ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	-32	V
Collector-base voltage	V_{CBO}	-45	V
Emitter-base voltage	V_{EBO}	-6	V
Continues collector current [a]	I_C	-3	A
Continues collector current [b]		-2	A
Pulse collector current [c]	I_{CM}	-6	A
Power dissipation [a]	P_D	3.0	W
Power dissipation [b]		1.2	W
Junction Temperature	T_J	150	°C
Lead Temperature	T_L	260	°C
Storage Temperature Range	T_{stg}	-55~155	°C

a Surface mounted on FR-4 Board using 1 square inch pad size, 1oz copper

b Surface mounted on FR-4 board using minimum pad size, 1oz copper

c Pulse width=300μs, Duty Cycle<2%

Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Collector-emitter breakdown voltage	BV_{CEO}	I_C=-10mA, I_B=0mA	-32			V
Collector-base breakdown voltage	BV_{CBO}	I_C=-1mA, I_E=0mA	-45			V
Emitter-base breakdown voltage	BV_{EBO}	I_E=-100uA, I_C=0mA	-6			V
Collector cutoff current	I_{CBO}	V_{CB}=-40V			-100	nA
Emitter cutoff current	I_{EBO}	V_{EB}=-5V			-100	nA
Collector-emitter saturation voltage [c]	$V_{CE(sat)}$	I_C=-2A, I_B=-200mA		-0.2	-0.5	V
Base-emitter saturation voltage [c]	$V_{BE(sat)}$	I_C=-2A, I_B=-200mA		-1.0	-1.5	V
DC current gain [c]	h_{FE}	IC=-1A , VCE=-2V	100	200	320	

4-1-5. NAND+SDRAM(U401)

1. FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 162ball FBGA Type - 11.5 x 13 x 1.0mmt, 0.5mm pitch

<e·MMC>
• embedded MultiMediaCard Ver. 5.0 compatible. Detail description is referenced by JEDEC Standard
• SAMSUNG e·MMC supports features of eMMC5.0 which are defined in JEDEC Standard
- Supported Features : Packed command, Cache, Discard, Sanitize, Power Off Notification, Data Tag, Partition types, Context ID, Real Time Clock, Dynamic Device Capacity, HS200
- Non-supported Features : Large Sector Size (4KB)
• Additional features of eMMC5.0 : HS400 mode (200MHz DDR - up to 400Mbps), Field Firmware Update, Device Health Report, Sleep Notification, Secure Removal Type
• Full backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-e·MMC systems)
• Data bus width : 1bit (Default), 4bit and 8bit
• MMC I/F Clock Frequency : 0 ~ 200MHz
MMC I/F Boot Frequency : 0 ~ 52MHz
• Power : Interface power → VDD = VCCQm(1.70V ~ 1.95V or 2.7V ~ 3.6V), Memory power → VDDF = VCCm(2.7V ~ 3.6V)

<LPDDR2>
• Double-data rate architecture; two data transfers per clock cycle
• Bidirectional data strobes (DQS, $\overline{DQS}$), These are transmitted/ received with data to be used in capturing data at the receiver
• Differential clock inputs (CK and $\overline{CK}$)
• Differential data strobes (DQS and $\overline{DQS}$)
• Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
• 8 internal banks for concurrent operation
• Data mask (DM) for write data
• Burst Length: 4 (default), 8 or 16
• Burst Type: Sequential or Interleave
• Read & Write latency : Refer to Table 47 LPDDR2 AC Timing Table
• Auto Precharge option for each burst access
• Configurable Drive Strength
• Auto Refresh and Self Refresh Modes
• Partial Array Self Refresh and Temperature Compensated Self Refresh
• Deep Power Down Mode
• HSUL_12 compatible inputs
• VDD1/VDD2/VDDQ/VDDCA
: 1.8V/1.2V/1.2V/1.2V
• No DLL : CK to DQS is not synchronized
• Edge aligned data output, center aligned data input
• Auto refresh duty cycle : 3.9us
• 2/CS, 2CKE

Items		4Gb
Device Type		S4
Number of Banks		8
Bank Addresses		BA0-BA2
t_{REFI}(us)*2		3.9
x32	Row Addresses	R0-R13
	Column Addresses*1	C0-C9

2. GENERAL DESCRIPTION

The KMK5X000VM is a Multi Chip Package Memory which combines 4GB e·MMC and 8Gbit DDP LPDDR2 S4 SDRAM.

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.41 which is a industry standard.
e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.
There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.
The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

LPDDR2-S4 uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.Prior to normal operation, the LPDDR2 must be initialized.

The KMK5X000VM is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 162-ball FBGA Type.

3. PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	DAT0m	DAT6m	VDD1m	DAT5m	DAT3m	VCCm	DNU	DNU
B	DNU	VCCm	DAT1m	DAT7m	CLKm	DAT4m	DAT2m	VCCQm	VSSm	DNU
C	RSTm	VCCQm	VSSQm	RCLKm	CMDm	VSSQm				
D	NC	NC	NC	NC	NC	NC				
E	VSSm	NC	NC		VDD2e	VDD1e	DQ31e	DQ29e	DQ26e	DNU
F	VDD1e	VSSe	NC		VSSe	VSSQe	VDDQe	DQ25e	VSSQe	VDDQe
G	VSSe	VDD2e	ZQe		VDDQe	DQ30e	DQ27e	DQS3e	$\overline{DQS3}$e	VSSQe
H	VSSCAe	CA9e	CA8e		DQ28e	DQ24e	DM3e	DQ15e	VDDQe	VSSQe
J	VDDCAe	CA6e	CA7e		VSSQe	DQ11e	DQ13e	DQ14e	DQ12e	VDDQe
K	VDD2e	CA5e	Vref(CA)e		$\overline{DQS1}$e	DQS1e	DQ10e	DQ9e	DQ8e	VSSQe
L	VDDCAe	VSSe	$\overline{CK}$e		DM1e	VDDQe				
M	VSSCAe	NC	CKe		VSSQe	VDDQe	VDD2e	VSSe	Vref(DQ)e	
N	CKE0e	CKE1e	NC		DM0e	VDDQe				
P	/CS0e	/CS1e	NC		$\overline{DQS0}$e	DQS0e	DQ5e	DQ6e	DQ7e	VSSQe
R	CA4e	CA3e	CA2e		VSSQe	DQ4e	DQ2e	DQ1e	DQ3e	VDDQe
T	VSSCAe	VDDCAe	CA1e		DQ19e	DQ23e	DM2e	DQ0e	VDDQe	VSSQe
U	VSSe	VDD2e	CA0e		VDDQe	DQ17e	DQ20e	DQS2e	$\overline{DQS2}$e	VSSQe
V	VDD1e	VSSe	NC		VSSe	VSSQe	VDDQe	DQ22e	VSSQe	VDDQe
W	DNU	NC	NC		VDD2e	VDD1e	DQ16e	DQ18e	DQ21e	DNU
Y	DNU	DNU							DNU	DNU

162FBGA: Top View (Ball Down)

4. PIN DESCRIPTION

Pin Name	Pin Function (e-MMC)
DAT0m – DAT7m	Data Input/Output
CLKm	Clock
RCLKm	Data Strobe
CMDm	Command
VCCm	Power Supply for Flash
VCCQm	Power Supply for Controller
VDDIm	External capacitance for Internal power stability
VSSm	Ground for Controller/Flash
VSSQm	I/O Ground
RSTm	Reset

Pin Name	Pin Function
NC	No Connection
DNU	Do Not Use

Pin Name	Pin Function (LPDDR2)
CKe, $\overline{CK}$e	System Differential Clock
CKE0e, CKE1e	Clock Enable
$\overline{CS0}$e, $\overline{CS1}$e	Chip Selection
CA0e – CA9e	Command / Address Inputs
DM0e – DM3e	Input Data Mask
DQS0e – DQS3e	Data Strobe Bi-directional
$\overline{DQS0}$e – $\overline{DQS3}$e	Data Strobe Complementary
DQ0e – DQ31e	Data Inputs / Output
VDD1e	Core Power Supply 1
VDD2e	Core Power Supply 2
VDDCAe	Input Receiver Power Supply
VDDQe	I/O Power Supply
VREF(CA)e	Reference Voltage for CA Input Receiver
VREF(DQ)e	Reference Voltage for DQ Input Receiver
VSSe	Ground
VSSCAe	Ground for CA Input Receivers
VSSQe	I/O Ground
ZQe	Reference Pin for Output Drive Strength Calibration

5. ORDERING INFORMATION

KM K 5 X 0 0 0 V M - B 314

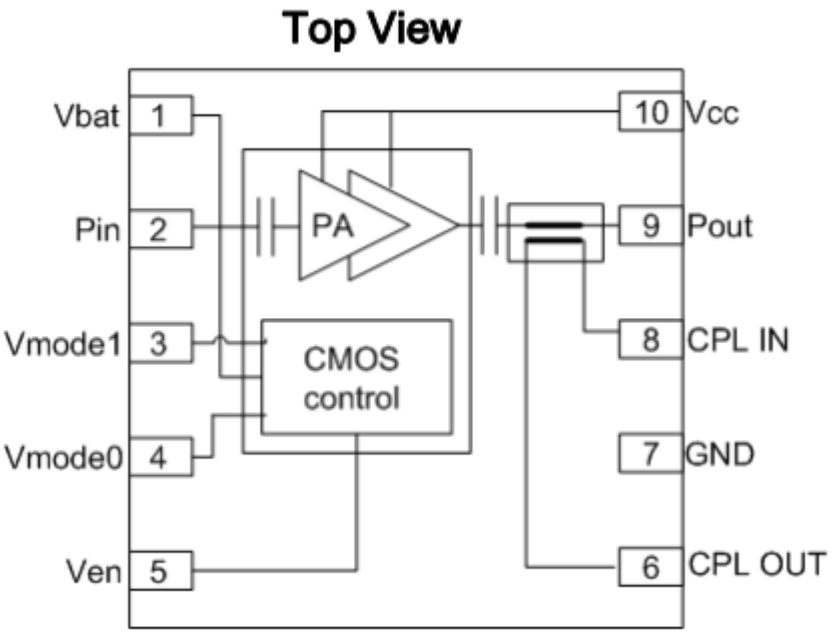
- KM — Samsung MCP Memory(5chips)
- K — Device Type: K : e-MMC + LPDDR2 SDRAM+ LPDDR2 SDRAM
- 5 — e-MMC Density, VCC,Org.: 5: 4Gbyte, 32G, TLC, 3.3V, 1.8V~3.3V, x8
- X — LSI: X : VPX01_PWD
- 0 — NOR Flash Density, VCC, Org.: 0 : NONE
- 0 — NAND/OneNAND Density,VCC, Org.: 0 : NONE
- 0 — UtRAM/SRAM Density,VCC, Org.: 0 : NONE
- V — DRAM Interface Density,VCC, Org.: V: LPDDR2*2, 4G*2,1.8V/1.2V, x32
- M — Version: M : 1st Generation
- B — Package: B : FBGA(HF, OSP LF)
- 314 — Access Time: 314: 6ns,1.9ns, 1.9ns

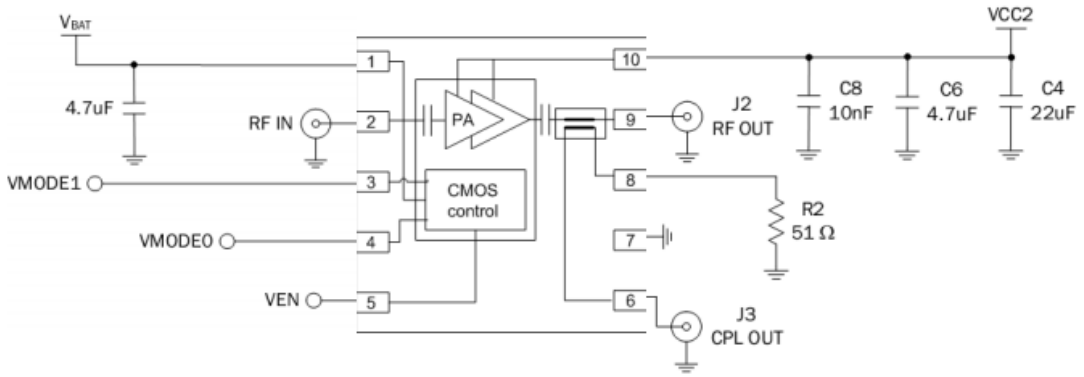
4-2. RF part

4-2-1 RF PA(U101)

Features

- 3.2 to 4.2V low voltage bias power supply
- Support for WCDMA/HSDPA/HSUPA
- The linear output power to 28 DBM
- 45% efficient (28 DBM)
- Provide three gain modes
- For using DC/DC power supply and optimization
- Built-in power coupler
- Integration of input and output isolation condenser
- For WCDMA B1 handsets and data CARDS
- Small package:3*3*1.0mm
- The main process：HBT/COMS





4-2-2. RF TRANSCEIVER (U201)

Introduction

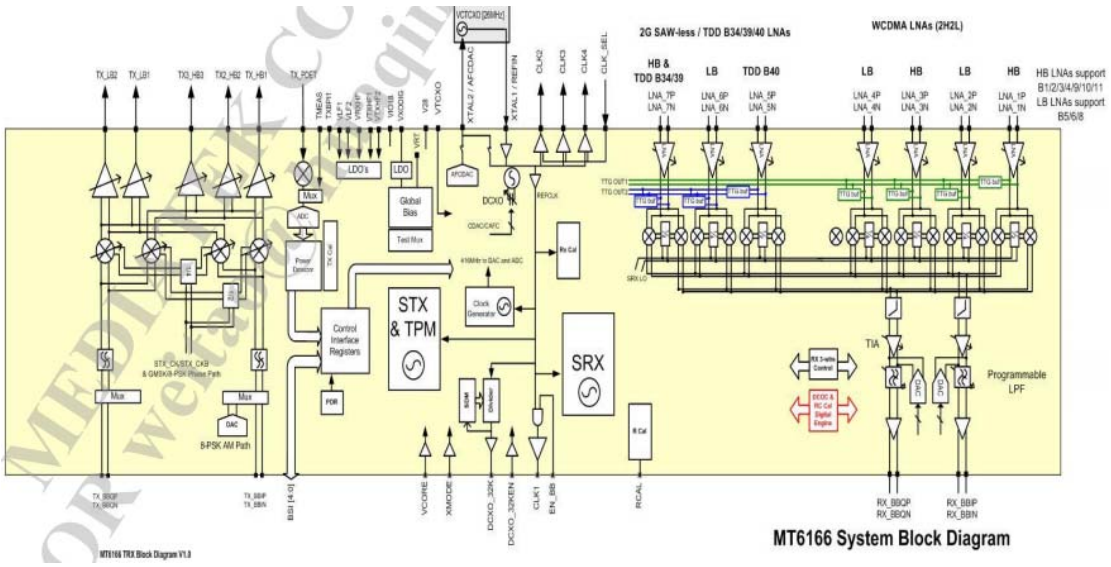
Overview

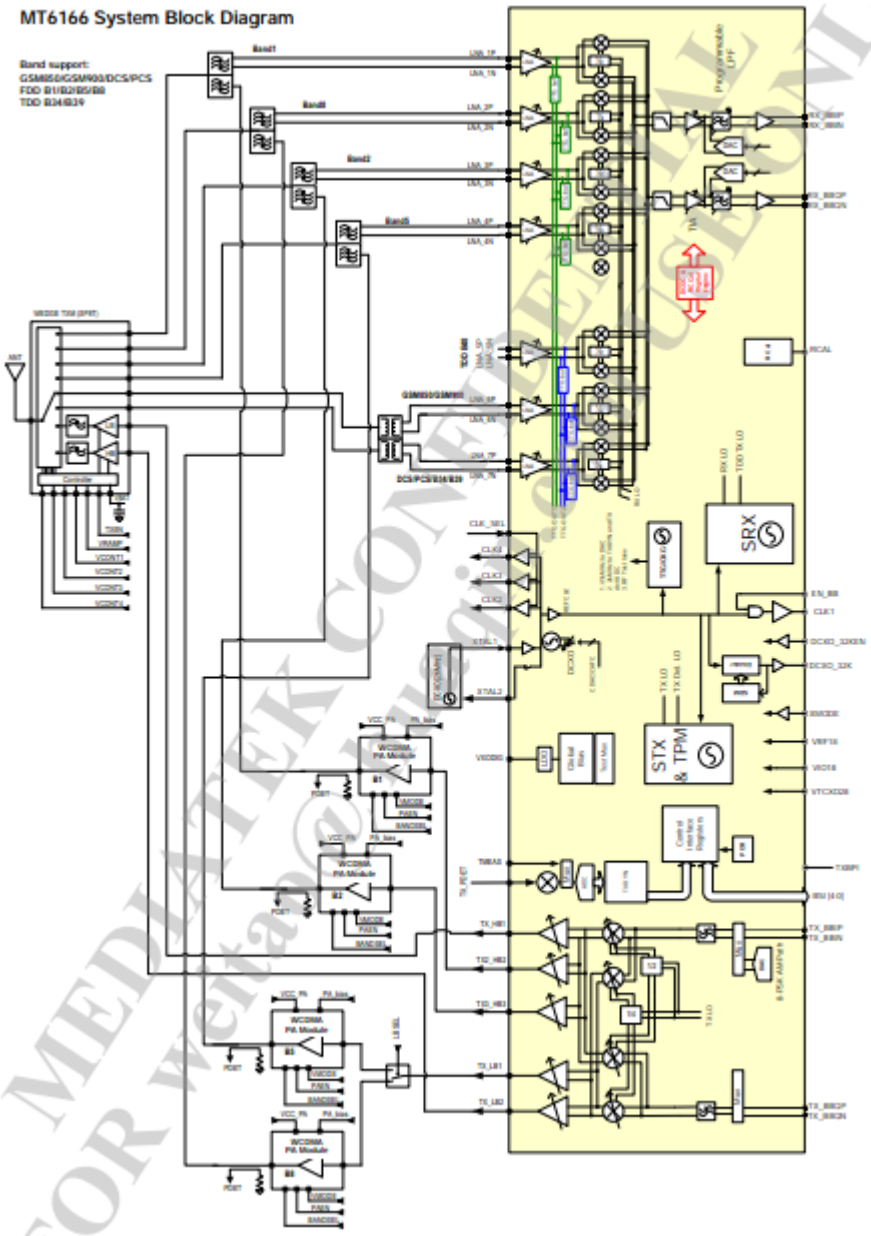
The MT6166 is a RF transceiver targeted at high speed 2G/3G-FDD/TDD multi-mode smart phone and tablet computers implanted in 40nm CMOS. The RF transceiver function is fully integrated. This document briefly introduces the RF macros in MT6166.

Key features

- Full multi-mode RF solution (GGE/WCDMA/TDSCDMA) through to 3GPP Release 8 (HSPA+)
  - 21.1Mbps peak DL (Cat. 24: 64QAM)
  - 11.5Mbps peak UL (Cat. 7: 16QAM)
  - SAW-less Quad-band support in GGE mode (GSM850/900/1800/1900)
  - 3G-FDD bands support: Band 1,2,5,8.
  - 3G-TDSCDMA bands support: Band 34,39,40.
- Direct Conversion (3G), Two Point Modulation (TPM) for GMSK and Small Signal Polar for 8-PSK
  - No external SAW filters required for transmitter (WCDMA//GGE)
  - Dedicated power detection circuits for power control over specific power range
- Hybrid Direct-Conversion (3G) / Low-IF (GGE, DC-HSDPA) receiver
  - No external SAW filters required for receiver (GGE)
- Low supply current & operation directly from DC-DC converter
- 26MHz internal DCXO or external VCTCXO operation (with integrated AFC DAC)
  - Three low noise additional Clock Drivers for clocking connectivity / peripheral IC's
  - Ultra Low power 32KHz mode
- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feedthrough, DC offset)
- Temperature Measurement sub-system

Block Diagram and Application Diagram





Ball assignment

	1	2	3	4	5	6	7	8	9	10	11	
A	B40_RXP	3GB1_RXP	3GB1_RXN		3GB2_RXP	3GB8_RXP		3GH1_TX	3GH2_TX	3GL5_TX	2GLB_TX	A
B	B40_RXN		3GB5_RXP	3GB5_RXN	3GB2_RXN	3GB8_RXN	GND	2GHB_TX		GND	VTXHF	B
C	LB_RXP	GND	GND	GND	GND	GND	GND	GND	GND	GND	TMEAS	C
D	LB_RXN		GND	GND	GND	GND	GND	GND	GND	DETGND	DET	D
E	HB_RXP		GND	GND	GND	GND	GND	GND	GND	V28		E
F	HB_RXN	VRXHF	GND	GND	GND	GND		BSI_DATA0	GND	3GTX_QP	3GTX_QN	F
G	32K_EN	RFVCO_MON	GND	GND		BSI_EN		BSI_DATA2	GND	3GTX_IP	3GTX_IN	G
H		XTAL2	GND	GND		BSI_CLK		BSI_DATA1	GND	TXBPI		H
J	XTAL1	GND	GND	GND	GND	GND	GND	GND	GND	RCAL	VTXLF	J
K	VTCXO28	CLK_SEL	XO2	XO4	OUT32K	AVDD_VIO18	VXODIG	RX_IN	RX_QN	RX_QP	TST2	K
L	EN_BB	XO3		XO1	XMODE		VRXLF	RX_IP		TST1	TXVCO_MON	L
	1	2	3	4	5	6	7	8	9	10	11	

RF I/O list

Category	Ball Name			Description
	Name	I/O	GPIO/RF Pin	
RF I/O	HB_RXP	I	RF	2G RX HB/TDD B34/39 input
	HB_RXN	I	RF	2G RX HB/TDD B34/39 input
	LB_RXP	I	RF	2G RX LB input
	LB_RXN	I	RF	2G RX LB input
	RFIN_B1	I	RF	3G band 1 RX input
	RFIP_B1	I	RF	3G band 1 RX input
	RFIN_B5	I	RF	3G band 5 RX input
	RFIP_B5	I	RF	3G band 5 RX input
	RFIN_B2	I	RF	3G band 2 RX input
	RFIP_B2	I	RF	3G band 2 RX input
	RFIN_B8	I	RF	3G band 8 RX input
	RFIP_B8	I	RF	3G band 8 RX input
	B40_RXP	I	RF	TDSCDMA Band 40 RX input
	B40_RXN	I	RF	TDSCDMA Band 40 RX input
	2GHB_TX	O	RF	2G HB TX output
	3GH1_TX	O	RF	3G HB TX output 1
	3GH2_TX	O	RF	3G HB TX output 2
	3GL5_TX	O	RF	3G LB TX output
	2GLB_TX	O	RF	2G LB TX output
	DET	I	RF	TX detection path input
BB I/O	3GTX_IP	I	RF	TX I+ input from 3G DAC
	3GTX_IN	I	RF	TX I- input from 3G DAC
	3GTX_QP	I	RF	TX Q+ input from 3G DAC
	3GTX_QN	I	RF	TX Q- input from 3G DAC
	RX_IP	O	RF	RX I+ ouput to 2G/3G ADC
	RX_IN	O	RF	RX I- ouput to 2G/3G ADC
	RX_QP	O	RF	RX Q+ ouput to 2G/3G ADC
	RX_QN	O	RF	RX Q- ouput to 2G/3G ADC
	TMEAS	I	RF	External temperature measurement input
	TXBPI	O	GPIO	3G TX DCOC sign bit
BSI Interface	BSI_CLK/SCAN_CLK	I	GPIO	3-wire CLK / ATPG CLK
	BSI_EN/SCAN_EN	I	GPIO	3-wire enable / ATPG enable

	BSI_DATA0/SCAN_IN	IO	GPIO	3-wire data/2G data / ATPG input
	BSI_DATA1/SCAN_OUT	IO	GPIO	3-wire data/2G data / ATPG output
	BSI_DATA2	IO	GPIO	3-wire data/2G data
TCVCXO/DCXO	XTAL1	I	RF	XO input
	XTAL2/AFCDAC	IO	RF	XO input or AFCDAC voltage output
	XO4	O	RF	26MHz output clock 4 (PMIC/Audio)
	XO3	O	RF	Sine-26MHz output clock 3 (ATV/NFC)
	XO2	O	RF	26MHz output clock 2 (CON)
	XO1	O	RF	26MHz output clock 1 (BB/AP)
	XMODE	I	RF	DCXO(=1)/VCTCXO(=0) selection.
	CLK_SEL	I	RF	XO output buffer (for co-clock) enable
	32K_EN	I	RF	32KHz function enable (with 32KHz XO, EN=0; without 32KHz XO, EN=1)
	OUT32K	O	RF	32KHz output
	EN_BB	I	RF	Enable 26MHz clock buffer to DBB. Also to be the enable of global static macro.
Test / RCAL Ports	TST1	O	RF	Test output 1
	TST2	O	RF	Test output 2
	RCAL	O	RF	R-calibration
VCO Mon	RXVCO_MON	O	RF	Monitor port for RFVCO.
	TXVCO_MON	O	RF	Monitor port for TX VCO.
Voltage Supply /GND	DETGND	GND	RF	For TX Pdet GND (50-ohm R GND)
	VRXHF	VDD	RF	1.8V RX power supply1 (VRF18)
	AVDD_VIO18	VDD	RF	1.8V DC-DC power supply (=VGPIO, only for GPIO supply)
	VXODIG	VDD	RF	For DCXO digital and GS supply, connect to VTCXO28 with 32k-removal, connect to VIO18 for normal operation. (=VIO18 in original plan)
	VTCXO28	VDD	RF	2.8V LDO XO power supply and BG
	VRXLF	VDD	RF	1.8V RX power supply2 (VRF18) and TTG/CKG
	VTXLF	VDD	RF	1.8V TX power supply 2 (VRF18)
	VTXHF	VDD	RF	1.8V TX power supply 1 (VRF18)
	V28	VDD	RF	For ESD and TX some blocks supply

Operating Conditions

Parameter	Conditions	Min	Nom	Max	Unit
Supply VIO18	Normal functional modes	1.7	1.8	1.9	V
Linear Supply VTCXO28		2.7	2.8	2.9	V
Supply VXODIG	Normal function mode	Connects to VIO18			
Supply VXODIG	32K-less mode	Connects to VTCXO28			
Supply VXODIG	ATPG mode – LDO's bypassed in this mode	1.1	1.2	1.4	V
Ambient Temperature	Note 1	-40		85	℃
Junction Temperature	Functional – see section [3.9]	-40		125	℃
Receiver Front End					
RX input frequency range	See Receiver Section for detailed frequency ranges				
Rx required amplitude balance	All Rx input pairs	-1		+1	dB
Rx required phase balance	All Rx input pairs	-10		+10	deg
Transmitter					
Tx Frequency Range	See Transmitter Section for detailed frequency ranges				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	
Reference Clock Input (VCTCXO)					
Reference Clock Frequency			26.0		MHz
Reference Clock Input Voltage Swing	AC coupled at input pin	700		1500	mVpp
Duty Cycle		40		60	%
Phase Noise – note 2	@ F_{offset} = 100Hz		<-103	-100	dBc/Hz
	@ F_{offset} = 1KHz		<-133	-130	dBc/Hz
	@ F_{offset} = 10KHz		<-147	-144	dBc/Hz
	@ F_{offset} = 100KHz		<-149	-146	dBc/Hz
Harmonic Content	HD2 @ 52MHz			-8	dBc
	HD3 @ 78MHz			-10	dBc
	HD4 @ 104MHz			-20	dBc
Start-up time	|Δf|<1ppm to >90% of final amplitude			3	ms
Crystal Requirements					

2 Crystal types are supported (Crystal #1 3225 body size / Crystal #2 2520 body size)					
Nominal Load Capacitance	Crystal #1		7.5		pF
	Crystal #2		7.0		pF
Initial Frequency error				±10	Ppm
ESR				30	Ω
Drive level				100	μW
Pull ability	Crystal #1	-10%	32	+10%	ppm/pF
	Crystal #2	-10%	27	+10%	ppm/pF

Note 1

The supportable ambient temperature range will depend on the thermal impedance of the package used and the exact operational state as well as the end application thermal design (housing, PCB etc).

Junction temperature is a more reliable indication of the actual operational range.

Note 2

The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements e.g. IC EVM specification. Certain connectivity requirements may require better specifications than this. The clock source (non DCXO mode) can either be an external VCTCXO/VCXO module or alternatively another transceiver clock buffer when considering multiple transceiver applications.

5. Test Instructions

Press the volume down button and power button to enter the engineering test mode, select "full test" into automatic test pattern:

1. ALS/PS test;
2. Touch Panel test;
3. LCD test;
4. LCD Back Light test;
5. Receiver test;
6. Speaker test;
7. KeyPad and Vibrating test;
8. Main MIC test;
9. Headset test;
10. FM Radio test;
11. SIM detect test;
12. T-flash Card test;
13. G-sensor test;
14. Wifi test;
15. BlueTooth test;
16. GPS test;
17. Battery & Charge test;
18. Version test;
19. Back Camera +Torchled test;
20. Front Camera test;
21. RTC test

6. Glossary

Term	Description
A3	Algorithm 3, authentication algorithm; used for authenticating the subscriber
A38	A single algorithm performing the functions of A3 and A8
A5	Algorithm 5, cipher algorithm; used for enciphering/deciphering data
A8	Algorithm 8, cipher key generator; used to generate K_c
AFC	Automatic Frequency Control
AFE	Analog Front End
AGC	Automatic Gain Control
AHB	ARM Host Bus
ALU	Arithmetic Logic Unit
AMR	Adaptive Multi-Rate. Speech and channel coding capable of operating at 11.4 kbps (Half-Rate) or 22.8 kbps (Full-Rate), and at some combination of speech and channel coding (codec mode).
APB	Advanced Peripheral Bus (part of AMBA)
BCCH	Broadcast Control CHannel
BTS	Base Transceiver Station
CCA	Convolution Coding Accelerator
CI	Command Interpreter—AT commands
CTM	Cellular Text Mode (TTY)
CVSD	Continuously Variable Slope Delta Modulation (codec)
DAC	Digital to Analog Converter
DAI	Digital Audio Interface
DMA	Direct Memory Access
DMAC	DMA Controller
DRM	Digital Rights Management
DRX	Discontinuous Reception
DTX	Discontinuous Transmission
EMC	External Memory Controller
FCA or FCCP	Fire-Cipher Accelerator
FCB	Frequency Control Burst
FEC	Forward Error Correction
GKI	Generic Kernel Interface. TTPCom operating system abstraction interface.
GPIO	General Purpose I/O
GPSR	General Purpose Shift Register (I^2C)
GSM	Global System Mobile

Term	Description
HCLK	Main EMC clock and AHB synchronous clock
IMEI	International Mobile Equipment Identity
IMSI	International Mobile Subscriber Identity
LLC	Logical Link Control
MCU	Microcontroller Unit. For the Si4901, MCU = ARM core.
MIDI	Musical Instrument Digital Interface
MMA	MIDI Manufacturer's Association
MS	Mobile Station—Handset
NLMS	Normalize Least Mean Square
NVRAM	Non-Volatile RAM
OMA	Open Mobile Alliance
OPLL	Offset Phase Lock Loop
OS	Operating System
OTP	One Time Programmable
PA	Power Amplifier
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PLMN	Public Land Mobile Network
PMU	Power Management Unit
POCO	Power Control Module
PPP	Point to Point Protocol
PROM	Program Read-Only Memory
RATSCCH	Robust AMR Traffic Synchronized Control Channel. This channel is used, like FACCH, to pass signaling associated with the AMR traffic channel.
RLC	Radio Link Control
RSA	An public-key encryption technology developed by RSA Data Security, Inc. The acronym stands for Rivest, Shamir, and Adelman, the inventors of the technique.
RSSI	Received Signal Strength Indication. The mean square amplitude of a block of samples following dc removal. It is expressed in fractional dB units.
RTC	Real-Time Clock
RTEC	Real-Time Event Controller
RTTTL	Ringing Tones Text Transfer Language, also known as Nokring. This ring tone format was first introduced on the Nokia phones and the format has become a standard for transfer and publishing of ring tones on the Internet
SCC	Slow Clock Calibration
SID	Silence Indication (Frame)
SIM	Subscriber Identification Module
SLAB	Silicon Laboratories®, Inc.

Term	Description
SMC	Sleep Mode Controller
SMS	Short Message Service
SSI	Synchronous Serial Interface
TCM	Tightly Coupled Memory
TTY	Tele-Type Terminal
TX VCO	Transmit Voltage-Controlled Oscillator (VCO)
VAD	Voice Activity Detection
VCM	Virtual Common Mode
VCP	Viterbi Coprocessor
WIM	WAP Identity Module

7. Warnings and cautions

Warnings

- If the device can be installed in a vehicle, Care must be taken on installation in vehicles fitted with. Electronic engine management systems and anti-skid braking systems. Under certain fault conditions, Emitted rf energy can affect their operation. If necessary, Consult the vehicle dealer/manufacturer to determine the immunity of vehicle electronic systems to RF energy.
- The product must not be operated in areas likely to contain potentially explosive atmospheres, for example, Petrol stations(service stations),Blasting areas etc.
- Operation of any radio transmitting equipment, Including cellular telephones, May interferer with the functionality of inadequately protected medical devices. Consult a physician or the manufacturer of the menical device if you have any questions. Other electronic equipment may also be

subject to interference.

- Before making any test connections, Make sure you have switched off all equipment.

Cautions

- Servicing and alignment must be undertaken by qualified personnel only.
- Ensure all work is carried out at an anti-static workstation and that an anti-static wrist strap is worn.
- Ensure solder, wire, or foreign matter does not enter the telephone as damage may result.
- Use only approved components as specified in the parts list.
- Ensure all components, modules, screws and insulators are correctly re-fitted after servicing and alignment.
- Ensure all cables and wires are repositioned correctly.

ESD protection

- Any product of which the covers are removed must be handled with ESD protection. The SIM card can be replaced without ESD protection if the product is otherwise ready for use.
- To replace the covers ESD protection must be applied.
- All electronic parts of the product are susceptible to ESD. Resistors, too, can be damaged by static electricity discharge.
- All ESD sensitive parts must be packed in metallized protective bags

during shipping and handling outside any ESD Protected Area (EPA).

- Every repair action involving opening the product or handling the product components must be done under ESD protection.
- ESD protected spare part packages MUST NOT be opened/closed out of an ESD Protected Area.